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9 July 1981

NASA/Goddard Space Flight Center
Greenbelt, MD 20771

Attention: Mr. Denver Herr, Technical Officer, Code 810.1

Subject: Contract NAS5-25985, Final Project Report

References: (a) Item Sequence Number 4b2

(b) Material Inspection and Receiving Report (DD250) LKC0015 dated 2 April 1981

Gentlemen:

As contractually required by the above noted reference (a), LINKABIT hereby submits two (2) copies of the Final Project Report for the subject contract. The draft Final Project Report was approved by the above noted reference (b). This submittal completes LINKABIT's contractual obligations for the subject contract.

Also enclosed are three (3) copies of the related Material Inspection & Receiving Report (DD250). Request LINKABIT be provided with one (1) copy of the DD250 appropriately signed to indicate receipt and acceptance of this submittal.

Very truly yours,

Norman W. Stanley
Manager, Contracts

/deb

Enclosure: Final Project Report (2 copies)
DD250 (3 copies)

cc: ✓Graphic Arts Branch, Code 253 (1 reproducible copy)
Patent Counsel, Code 204 (1 copy)
Contracting Officer, Code 268.2 (1 copy)
DCAS/DCRL, Mr. Gary W. Thomas, ACO, San Diego, CA (1 copy DD250)

MATERIAL INSPECTION AND RECEIVING REPORT

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21. PROCUREMENT QUALITY ASSURANCE

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23. CONTRACTOR USE ONLY

FINAL REPORT

FOR

A SIMULATION SYSTEM FOR VALIDATING THE ANALYTICAL PREDICTION OF PERFORMANCE OF THE CONVOLUTIONAL ENCODED AND SYMBOL INTERLEAVED TDRSS S-BAND RETURN LINK SERVICE IN A PULSED RFI ENVIRONMENT

LINKABIT CORPORATION
3033 Science Park Road
San Diego, Ca. 92121

Table of Contents

1. INTRODUCTION

This report describes a hardware integrated convolutional coding/symbol interleaving and integrated symbol deinterleaving/Viterbi decoding simulation system which will be used by the government to validate the analytically predicted performance of the TDRSS S-band return link with BPSK modulation, operating in a pulsed RFI environment.

The system consists of three components, the Fast Linkabit Error Rate Tester (FLERT), the Transition Probability Generator (TPG), and a modified LV7017B which includes rate 1/3 capability as well as a periodic interleaver/deinterleaver. Operating and maintenance manuals for each of these units are included as appendices to this report.

The FLERT sends clocked psuedo-random data to the LV7017B, which encodes the data into symbols which are then interleaved and sent to the TPG. The TPG is programmed via an HP9825 calculator to simulate the statistics of various channels by inserting symbol errors and adding soft decision bits to the encoded and interleaved symbol stream. The corrupted symbol stream is returned to the LV7017B where it is deinterleaved and Viterbi decoded. The decoded data is sent to the FLERT, which measures the bit error rate and displays it. The HP9825 calculator is equipped with software that allows the user to run automated tests in which the operator loads pertinent parameters such as the required settings of the FLERT, the length of the test in bits, the location on cassette tape of the noise statistics to be used for the test, and the number of different

tests to be run. The calculator takes measurements from the FLERT and prints the results on its hard copy printer.

The LV7017B has a variety of modifications implemented for this particular application. The most significant of these is the addition of a reduced metric rate 1/3 capability. LINKABIT developed this metric by the use of computer simulations which determined the performance resulting from the use of each or four different metrics. The metric selected for use in this system exhibits performance within one-tenth of one dB of that of a non-reduced metric system. A summary of the results of LINKABIT's simulations is shown in the curves of Figure 1.1, which shows the performance of the four different cases simulated as well as that for the non-reduced metric case.

The modified LV7017B also contains a (30,116) periodic convolutional interleaver/deinterleaver which is integrated with the decoder to provide the best possible synchronization strategy. The decoder detects absence of synchronization by the rate at which path metrics grow in the decoding trellis. The deinterleaver is able to provide node synchronization to the decoder by using the knowledge that symbols from the "top tap" of the interleaver originated from code generator G1. Thus, when the decoder detects loss of sync, the deinterleaver takes the appropriate corrective action, and the decoder's internal synchronization is bypassed with the deinterleaver in the data path.

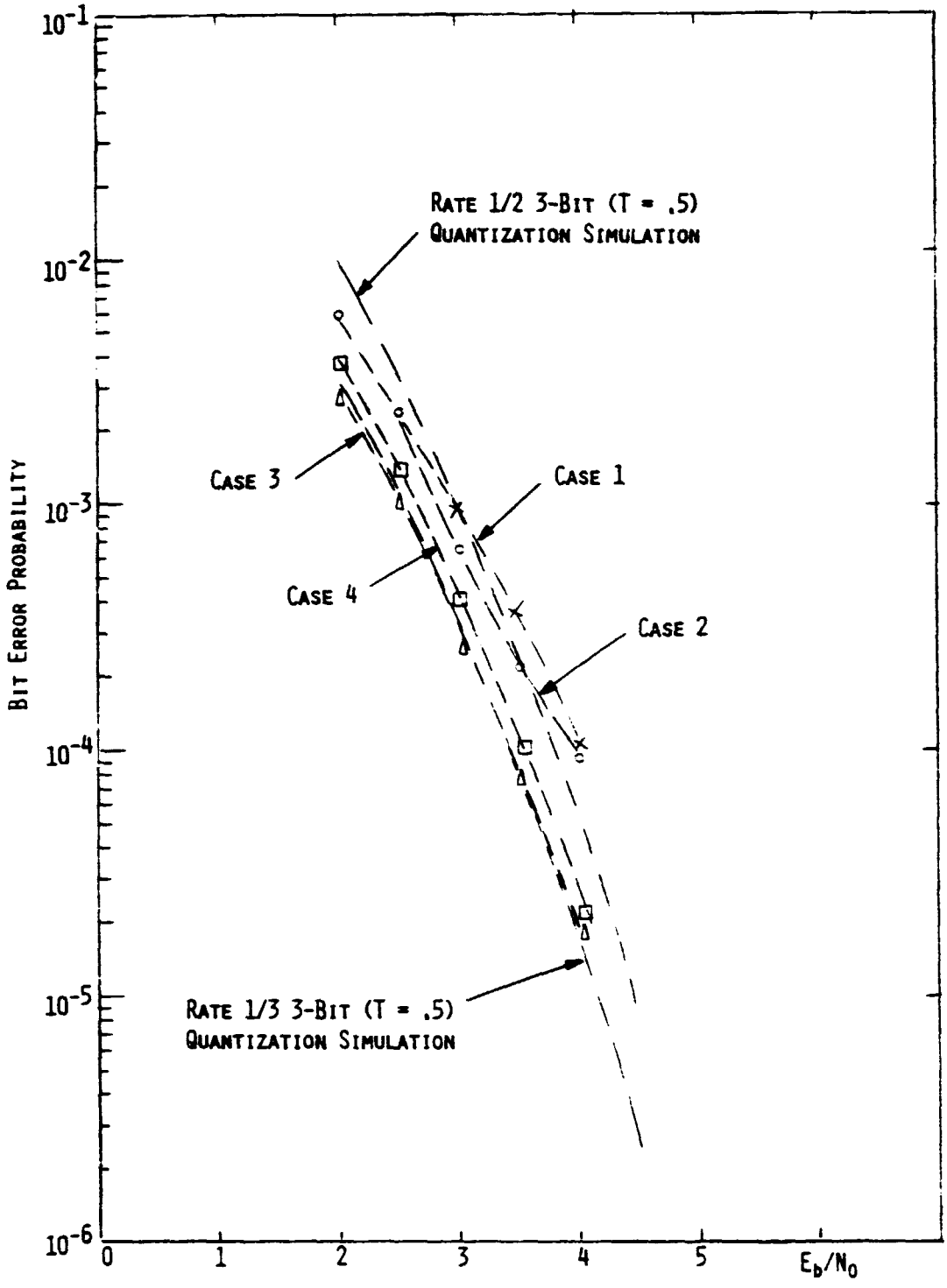


Figure 1.1 BER Performance of Rate 1/3 Metric Compression Schemes Compared With Rate 1/2 and 1/3 Performance.

2. DECODER PERFORMANCE

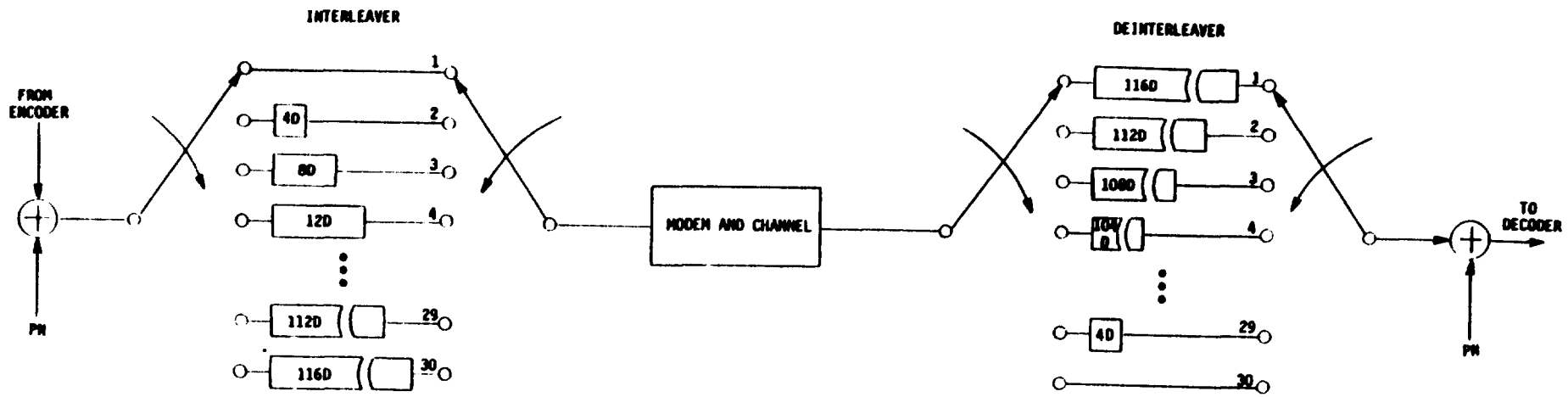
Decoder performance is summarized to some degree in the manual for the Modified LV7017B manual included as an appendix to this report. Performance in rate 1/2 is the same as that for LINKABIT's standard LV7017A or LV7017B. Rate 1/3 performance is degraded only slightly by the need to use a compressed metric due to the limitations of LINKABIT's LAM-40 chip. This degradation has been shown by simulation (see Figure 1.1) to be less than one tenth of one dB. Testing of the unit by LINKABIT indicates that the performance predicted by computer simulation is accurate. In particular, an exhaustive overnight test of the rate 1/3 performance at 4.1 dB yields an error rate of .00001091 which is within about .03 of one dB of the performance for the uncompressed metric case. During this test over 200,000 errors were recorded, so the confidence in the accuracy of the result is limited only by confidence in the accuracy of the TPG to produce exactly a 4.1dB distribution.

The presence of interleaving should have no effect on the performance of the decoder in the presence of wideband additive Gaussian noise, and this also has been measured to be the case.

3. INTERLEAVING -- THEORY OF OPERATION

The classical model for a (30,116) periodic convolutional interleaver/deinterleaver is shown in Figure 3.1. A PN cover sequence which repeats every 30 symbols is added to the incoming symbols, which are then multiplexed to the delay elements. The purpose of the PN sequence is to aid in synchronization. The "wiper" multiplexes the data between each of the 30 taps, moving one tap each symbol time in a periodic fashion. Each delay element provides a delay of four symbol times. The demultiplexing wiper tracks the multiplexing wiper.

When the interleaved stream of symbols is transmitted over a channel, it may be corrupted by the addition of bursts of noise. In the absence of interleaving, these bursts would have a catastrophic effect on the decoder, because the decoder is designed to correct random errors, but not blocks of errors. The process of deinterleaving has the effect of randomizing bursts of errors by returning the channel symbols to their original positions relative to each other. Any two bits in the interleaved data stream occurring within an inclusive sequence of 30 channel symbols will have at least 118 symbols between them in the deinterleaved data stream. This separation of symbols is greater than the memory of the decoder; thus bursts of less than 30 symbols are effectively randomized by the deinterleaving process. It should be noted that the two soft decision quality bits associated with each symbol produced by the modem must also be deinterleaved.



D = 1 SYMBOL DELAY

FIGURE 3.1 CLASSICAL PERIODIC CONVOLUTIONAL INTERLEAVER IMPLEMENTATION

4. DECODER/DEINTERLEAVER SYNCHRONIZATION STRATEGY

Deinterleaving synchronization is the process by which it is determined in which position the multiplexing and demultiplexing wipers should be placed for proper operation of the deinterleaver. By inspection, it is apparent that when the deinterleaver is in sync with the interleaver, each symbol encounters the same delay (116*30=3480 bit times) in passing through the combined interleaving/deinterleaving process; thus the only effect of using interleaving is to introduce a delay. When the deinterleaver is out of sync by, say, one tap delay with respect to the interleaver, the resulting symbol stream presented to the decoder, viewed in groups of 30 consecutive symbols, consists of 29 symbols all with the same delay (120*30=3600 symbol times) and 1 symbol with no delay. The decoder is able to decode such a sequence, albeit with much degraded performance. Thus a PN sequence is used to insure that when the deinterleaver is not in sync, the data presented to the decoder does not look like good data. This cover sequence is 30 bits long; one bit for each tap of the interleaver. The first bit of the sequence is exclusive OR'ed with the symbol coming out of the top tap of the deinterleaver, the second to the symbol from the second tap, and so on. Since this sequence is added to the symbol stream in the same fashion at the interleaver side, the PN sequence cancels itself out of the symbol stream when the unit is in sync, but when it is not in sync, the cover sequence makes the symbol stream look like pure noise, which makes the decoder signal loss of sync.

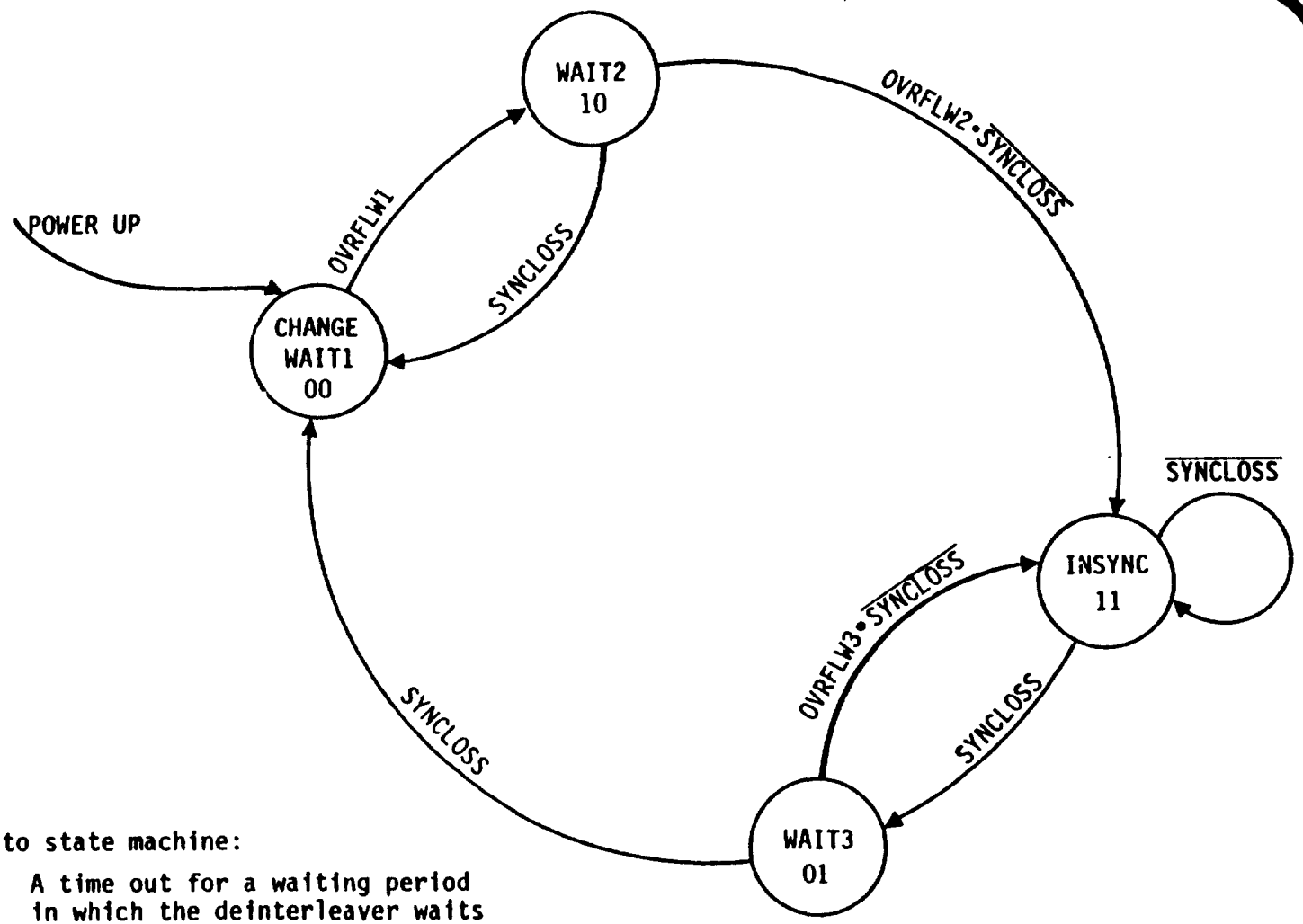
The sync strategy for the integrated decoder/deinterleaver,

shown in the state diagram of Figure 4.1, has been designed to minimize both the time needed to acquire sync (from either power up or an operating mode in which sync is lost) as well as the probability of changing sync state due to a false detection of sync loss. Upon power up, the deinterleaver enters the CHANGE/WAIT1 state in which the sync state is moved one state according to the spiral search strategy, illustrated in Figure 4.2. The spiral search is used because it is assumed that if sync is lost, the true sync state is near to the state currently occupied by the deinterleaver, so the states first to the left and then to the right are checked one by one until the correct state is found. After moving the sync state, the state machine waits for the period of time required to fill the deinterleaver RAM with good data. When this time has elapsed (as indicated by the occurrence of OVRFLW1) the state machine enters state WAIT2, where it waits to decide if the state chosen is correct. If a loss of sync is detected during this time, the state machine returns to state WAIT1 and changes sync state again.

The state machine declares the deinterleaver to be in sync if the time OVRFLW2 elapses without the occurrence of a loss of sync signal. It then proceeds to the INSYNC state, where it remains as long as no further loss of sync is detected. Should a sync loss be detected, the machine enters the state WAIT3, a state used to prevent false startup of the sync search, such as might occur if the Eb/No dropped to a low value for some period of time. The decoder might declare loss of sync due to the rapid growth of its metrics when the unit is actually in sync. If this event occurs, loss of sync will be declared only sporadically,

LINKABIT

FIGURE 4.1 DEINTERLEAVER SYNC SEARCH.



Two inputs to state machine:

1. OVRFLW: A time out for a waiting period in which the deinterleaver waits for a SYNCLOSS signal.
2. SYNCLOSS: A signal from the decoder indicating loss of sync.

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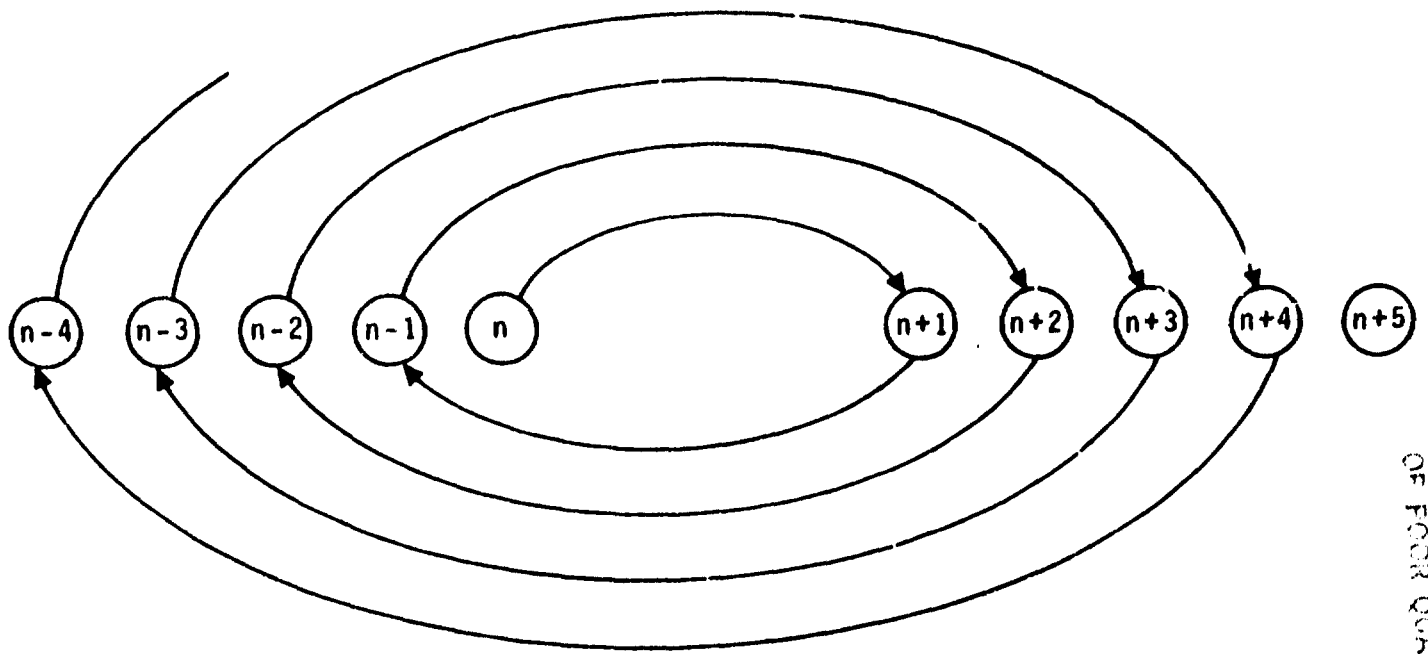
FIGURE 4.2 SPIRAL SYNC SEARCH.



and the OVRFLW3 counter will timeout before the next loss of sync signal is detected. When OVRFLW3 times out the machine returns to the INSYNC state.

If the state machine entered the state WAIT3 due to an actual loss of sync, the decoder will again signal loss of sync before OVRFLW3 times out. The state machine then moves to the CHANGE/WAIT1 state and begins its spiral search.

This synchronization strategy is very robust in many ways. It minimizes the likelihood that the deinterleaver falsely begins sync search due to low Eb/No operation, yet if a real loss of sync occurs it begins searching for the correct state in at most 1000 bit times. If the deinterleaver sync state is moved unsuccessfully, it takes only about 4000 bit times to detect this and move the sync state again. This is significant since 3600 symbol times must elapse just to fill the deinterleaver RAM so that the decoder is presented with properly deinterleaved data. With no overhead for the decoder to decide that sync has been lost, it would take 30*3600=108000 symbol times to cycle through all 30 sync states, just to have enough time to fill the deinterleaver RAM with good data at each state. Thus, the 120000 symbol times actually required for this process is only about 10% above the absolute minimum time in which the task could be performed.

5. DEINTERLEAVER SYNCHRONIZATION PERFORMANCE

The performance of the deinterleaver sync algorithm has been measured using the Transition Probability Generator and a logic analyzer. Initial sync time can be measured by loading the TPG with one state that produces an error rate of 50% and another that contains Gaussian noise with an Eb/No of 4.4 dB. The TPG starts out in the 50% noise state, and with some small probability P makes the transition to the 4.4 dB state, from which no transitions are allowed. The logic analyzer can be used to view when the TPG changes state and when the deinterleaver acquires the correct sync state, and measure the time between these events.

It is also a straightforward matter to estimate the time it should take to acquire initial sync. The dominant contributor to the sync time is the time it takes to fill the deinterleaver RAM -- 3600 symbol times. In addition to this there are at most 500 symbol times of overhead required for the decoder to determine that sync has not been acquired and for waiting in various states. Thus, a good estimate for the maximum time needed for each change of sync state is about 4000 symbols. In reality, this number is somewhat smaller because the decoder usually takes substantially less than 500 bit times to detect the out of sync condition. A typical Figure would be on the order of 150 to 200 symbol times. In the worst case, where the deinterleaver doesn't acquire sync until it tries the final sync state, it will take 30 states times 4000 symbols/state or 120,000 symbols to acquire sync. On the average, the deinterleaver will acquire initial sync on the fifteenth state attempted; thus the average initial

sync time will be 60,000 bit times. This number has been verified using a logic analyzer and the method described above.

Using a similar argument, it is obvious that the time required to recover sync when a single bit slip occurs will be a maximum of about 5000 symbols or 9000 symbols, depending on whether the deinterleaver sync circuit happens to begin its search in the same direction as the bit slip or if it looks the wrong way first. One thousand symbol times of this represents the time required to get from the INSYNC state to the CHANGE/WAIT1 state. Again, the real figure is generally much lower because the actual time to detect sync loss in the decoder is usually between 150 and 200 bit times. Thus the typical times for recovery from a single bit slip would tend to be closer to 4000 and 8000 symbol times. A switch in the TPG allows a bit slip to be introduced to the symbol stream so that this phenomenon may be observed, and the measured results are as predicted.

The most catastrophic sync loss occurs when the modem suffers a 180 degree phase reversal. This causes the symbol stream to be inverted. Without interleaving, this would present only a small problem to the decoder, which would make a short burst of errors and then produce inverted data at its output. (Or, if differential coding is used, after the burst of errors true sense data would again be output.) Unfortunately, the deinterleaving process mixes inverted symbols with non-inverted symbols and for a period of several thousand bit times presents the decoder with a sequence that has no resemblance to a code sequence. The decoder indicates loss of sync many times in succession, causing

the deinterleaver to start its sync search despite the fact that it is in the correct sync state. When this occurs, the deinterleaver must search all of its 30 states berore it returns to the correct state. Thus, inversion of the symbol stream causes a loss of about 120,000 symbols before sync is regained.

6. PERFORMANCE IN THE PRESENCE OF PULSED RFI

In studies [1,2] that LINKABIT performed on coding techniques for TDRSS in the presence of RFI that preceded this hardware development and in presentations of this work at NASA GSFC, several options for improving system performance were presented. In addition to rate 1/3, rather than rate 1/2, coding and the addition of interleaving/deinterleaving, transponder improvements such as limiter level setting and RFI detection and blanking at the receiver were described. One of the main reasons for suggesting the latter two improvements was to insure that with soft-decision decoding, a low confidence level (small quality) is assigned to the symbols received in the presence of RFI. If a small quality is not assigned to the RFI symbols, a significant performance degradation will occur. In fact, in such a situation hard decision decoding may be preferable to avoid giving the symbols with RFI an advantage over symbols not corrupted with RFI.

Since the synchronization strategy for the deinterleaver and decoder is based on the rate of growth of the Viterbi decoder path metrics, not assigning a small quality to the symbols with RFI will also degrade synchronization performance. In the Viterbi decoder implementation used here, the symbol metric assignment of Table 6-1 is used. With this metric assignment,

small metrics are considered good in the metric comparisons and on a very clean channel (large E_b/N_o, no RFI) the correct path would have a path metric of zero. The decoder tests for synchronization by observing the rate of growth of the path

Decoder Input Interval Designation	111	110	101	100	000	001	010	011
"+" Hypothesis Viterbi Decoder Symbol Metric (1)	4	3	2	1	0	0	0	0
"-" Hypothesis Viterbi Decoder Symbol Metric (1)	0	0	0	0	1	2	3	4
AWGN Positive Matched Filter Output Interval	$-\infty$ to -3Δ	-3Δ to -2Δ	-2Δ to $-\Delta$	$-\Delta$ to 0	0 to Δ	Δ to 2Δ	2Δ to 3Δ	3Δ to ∞

NOTES

(1) Compressed metrics are used and small metrics are considered good.

(2) Δ is a quantization parameter set equal to .5 times the standard deviation of the matched filter output.

TABLE 6-1: Viterbi Decoder Metric Assignments

metrics and if over some period of time this growth is greater than some threshold value, an out-of-sync indication is provided. In the decoder of this development, this synchronization threshold was set so that in the rate 1/2 mode with additive white Gaussian noise (AWGN) and E_b/N_o= 4.4 dB, the probability of detecting an out-of-sync condition after 500 channel symbols is .95. With this threshold setting AWGN induced loss of synchronizations cause no significant performance degradation for decoder output bit error rates of less than 10^{-1}.

When RFI is present and the symbols are received with the highest quality, the path metrics are increased by 4 (see Table 6-1) whenever the polarity of the Viterbi decoder hypothesized path and the received symbol disagree. Thus when such symbols are received the path metric increases at the same rate as for the AWGN out-of-sync channel with a large E_b/N_o. This increase in path metric growth rate increases the probability that an out-of-sync indication will incorrectly be announced. The synchronization performance can be adjusted by changing the sensitivity of the decoder to the rate of metric growth. However, even after synchronization, the performance will be severely degraded if symbols received in RFI are assigned a high quality. Also it is important to remember that increasing the sync time of the decoder will impact the sync time of the combined decoder and deinterleaver in such a way that an increase of 500 symbol times in the time needed for decoder sync acquisition alone will result in a worst case increase of 30 times 500 or 60,000 symbol times in the time needed for deinterleaver synchronization. The worst case deinterleaver sync

acquisition time for a single bit slip will go up by 500 or 1000 symbol times, depending on the direction of the slip.

Rather than adjusting the synchronization parameters to try to accomodate RFI symbols with high qualities, a better approach is to not assign high qualities to these symbols. For example, the RFI would be detected and these symbols assigned low qualities (i.e., blanking). Referring to the metric assignments of Table 6-1 that were used in this implementation, the RFI symbols would be assigned to one of the two center intervals with metrics of zero for either hypothesis. Then these symbols would not contribute to a path metric increase. In addition, with blanking, performance would be much better than when the symbols with RFI are assigned a high quality.

The integrated interleaver-decoder and its associated simulation test system developed under this contract is a very flexible vehicle for assessing the effects of mitigating techniques for channels distributed by significant RFI phenomena. As channel models are better understood and refined, this system will rapidly and reliably assess bit error rate performance of the link under consideration.

The Acceptance Test Procedure and Test Results are included in an appendix to this report.

REFERENCES

1. J.P. Odenwalder and A.J. Viterbi, "Final Report on RFI/Coding Sensitivity Analysis for Tracking and Data Relay Satellite System (TDRSS)," LINKABIT Corp., San Diego, CA, report submitted to ORI, Inc., Silver Spring, MD, 13 July 1978.

2. A.J. Viterbi, J.P. Odenwalder, I. Bar-David and K.M. Kumm, "Final Report on RFI/Coding Sensitivity Analysis for Tracking and Data Relay Satellite System (TDRSS) Phase II," LINKABIT Corp., San Diego, CA, report submitted to ORI, Inc., Silver Spring, MD, 12 January 1979.

FLERT II

OPERATING MANUAL

APPENDIX A

LINKABIT Corporation
a M/A-COM Company
3033 Science Park Road
San Diego, CA 92121

FLERT II
Operating Manual

Version 4.2

25 March 1981

Written By:
Ilan Peer
&
Steve Gardner

Table of Contents

Table of Figures

Section 1

About This Manual

This is an in-house manual describing the FLERT II theory and operation. Out-of-house users should regard this manual as a reference only.

Section 2

Theory of Operation

The Fast LINKABIT Error Rate Tester (FLERT) is a device used in the testing of digital communication systems. The FLERT generates pseudo-random data to be transmitted by the system and then compares the received data to that transmitted to determine the system bit error rate. The FLERT is capable of operating from 1 bps to 70 Mbps.

The FLERT generates data with a pseudo noise (PN) generator. This master generator consists of a 16-bit shift register and a parity checker which computes the parity of selected bits in the shift register. The result of this computation is then fed back to the input of the shift register (see Figure 2.1).

By selecting appropriate combinations of shift register bits with which to compute parity, many different sequences may be produced. The FLERT can produce maximal length PN sequences of length 2^n-1 for n = 4,8,11,15 and 16. It can also produce an all zero sequence and can invert any of these sequences prior to transmission.

Error rate computation is accomplished by comparing the received data to a PN sequence which is computed using the same bits of the shift register for computing parity as were used in generating the transmitted data (see Figure 2.2). This second PN generator must be "slaved" to the received data by means of synchronization circuitry. If the error rate exceeds 25% for a

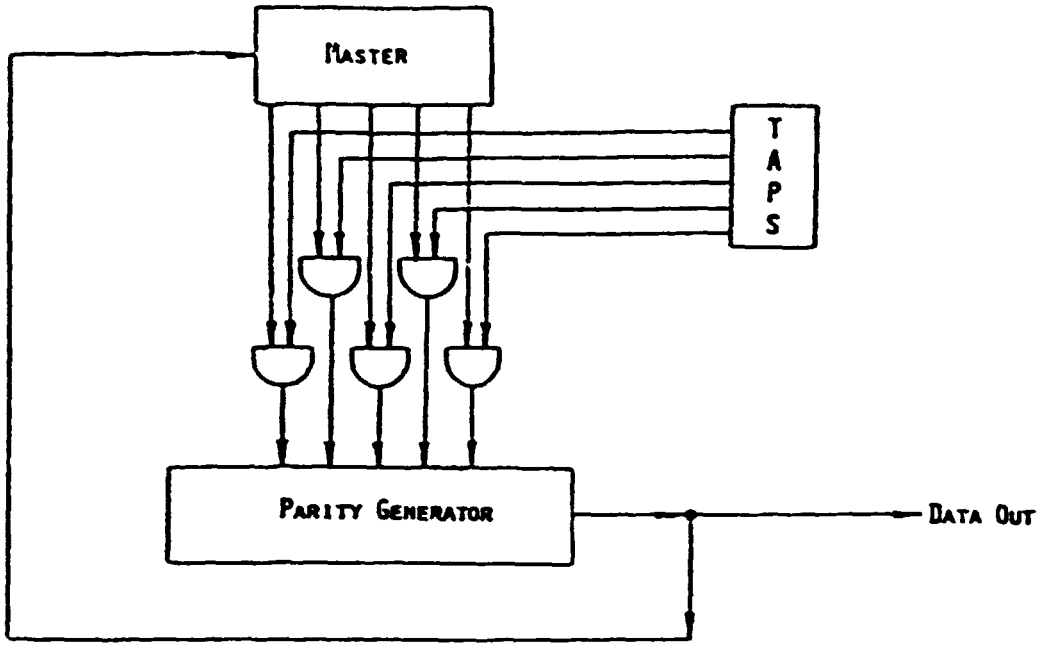


Figure 2.1. Master P/N Generator

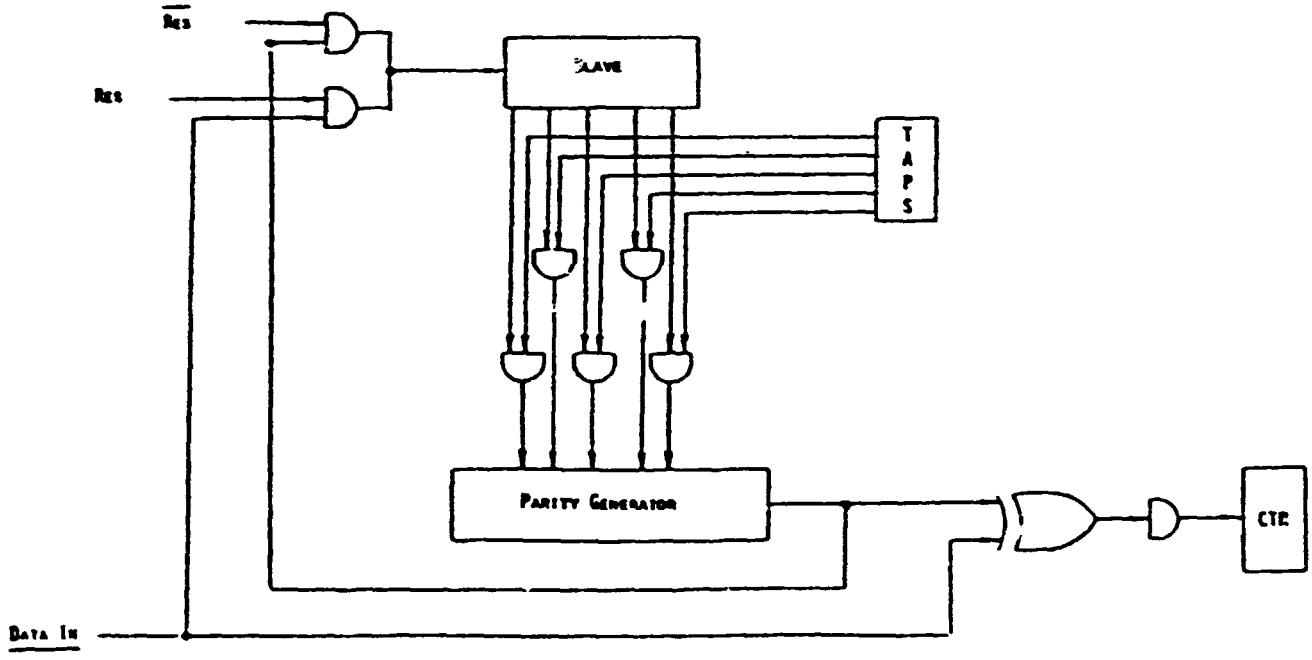


Figure 2.2. Slave P/N Generator

period of time, sync loss is assumed and the slave PN generator is resynchronized by using the received data, rather than the computed parity, as input to the shift register. When the shift register is filled with data bits, the output of the parity checker once again becomes the input to the shift register. If no errors occurred during resynchronization, the output of the parity checker will agree with the received data except where errors occur.

Loss of synchronization is detected by a two stage up/down counter which counts up one for each error and down for each four bit times. The counter is not allowed to count down through zero, and the transition from all ones up to all zeros is used to indicate loss of synchronization. One of two "rate integration thresholds" can be used. The low threshold causes resynchronization whenever the lower stage of the up/down counter counts up to all zeros regardless of the status of the upper stage. The high threshold causes resynchronization only when the upper stage counts up to all zeros.

The FLERT contains many other features besides the basic master/slave/synchronization circuitry. In the master, a counter detects the beginning of the PN sequence and produces a pulse called the scope sync which is available at the FLERT front panel. This signal is useful as a trigger for viewing data dependent phenomena on an oscilloscope.

The same counter also is used to start up the sequence. Should the master PN generator fall into an all zero state, a one

is fed into the shift register input to start up the sequence. If it is desired, one bit in a thousand out of the master may be inverted prior to output. This causes an error rate of 10^{-3} to appear at the slave.

Synchronization may be performed manually instead of automatically if desired. In manual sync mode the status of the rate integration counters is ignored except to darken the SYNC led when sync loss is detected.

Errors and bits are both counted and displayed by a Z80 microprocessor which also computes and displays the system bit error rate. The Z80 also controls all front panel and remote control functions.

A SYNTEST frequency synthesizer in the FLERT provides the user with a clock with programmable frequency from 1 Hz to 15.99 MHz.

Section 3

Interfaces

The FLERT has three types of interfaces - single ended TTL, differential TTL and differential ECL. The single ended TTL signals are terminated with 200 ohms to ground. The differential TTL inputs and outputs are type RS-422 (AM26LS31, AM26LS32 or equivalent) with 100 Ω termination. The differential ECL signals are typical 10K ECL drivers and receivers with 100 Ω termination. Differential ECL clock inputs are AC-coupled to allow use of a single ended clock source (such as a PTS-160) as well as differential ECL sources. The AC-coupling makes the ECL interface unsuitable for frequencies below 500 KHz.

The FLERT I/O consists of the following signals:

NAME	I/O	DESCRIPTION
MASTER CLK IN	I	Clock for master PN generator. Internal circuitry selects active edge and divides by 1,2 or 3.
CLK OUT	O	Data rate clock output.
DATA OUT	O	Master PN data output. Data changes within ± 20 ns of the rising edge of CLK OUT for TTL outputs and within ± 5 ns of the rising edge of CLK OUT for ECL.
SCOPE SYNC	O	Single ended ECL signal goes for one bit time at the end of the longest string of zeros in the selected PN sequence.

SEQUENCE RESTART INPUT SYNC	I	Active high signal places a one in the left most bit of the master shift register and zeros the others. Must be synchronous with CLK OUT. Not active if no connection is made.
SEQUENCE RESTART INPUT ASYNC	I	Same as above, but asynchronous.
SLAVE CLOCK IN	I	Data rate slave input clock. Active edge is user selectable.
DATA IN	I	Data signal from unit under test. Must be accompanied by a SLAVE CLK IN.
ERROR OUT	O	Active low signal goes low for one bit time whenever a bit error is detected.
GATED ERROR OUT	O	Active high signal goes high for one-half bit time whenever an error occurs and the gate is on (both gate button & error gate active).
ERROR GATE IN	I	Active low signal enables GATED ERROR OUT, auto synchronization circuit, bit and error counters when active. Signal is active if no connection is made.
INT CLK OUT	O	Internal clock output 1 Hz to 15.99 MHz as selected by user.
RS-232	I/O	RS-232 interface for remote control.
GPIB	I/O	GPIB (IEEE-488) interface for remote control.

Section 4

Front Panel Control

SWITCH	DESCRIPTION
PATTERN 2^4-1 2^8-1 $2^{11}-1$ $2^{15}-1$ $2^{16}-1$ ALL ZEROS	When button is lit the pattern indicated has been selected by the FLERT for both master and slave PN generators.
PATTERN INV	When button is lit the data output by the FLERT is inverted.
MASTER CLOCK + -	Lit button indicates the active edge of the input clock.
MASTER CLOCK ÷ 1 ÷ 2 ÷ 3	Lit button indicates data rate relative to input clock rate.
ERROR ADD	When lit, one error is introduced to the output data sequence each 1000 bits.
SLAVE CLOCK + -	Lit button indicates active edge of the input clock.
SLAVE AUTO MANUAL	Select automatic or manual synchronization of the slave PN generator as indicated by LED.

SLAVE SYNC	In AUTO mode, pushing button has no effect. in MANUAL mode, pushing the button causes resynchronization to be attempted. When the SYNC LED is lit, the slave PN generator is in SYNC. See SLAVE INV SYNC.
SLAVE INV SYNC	In AUTO mode pushing button has no effect but LED indicates whether input data is inverted or not (on = inverted data). In MANUAL mode, when on, the slave will attempt to synchronize with inverted data when SLAVE SYNC is pushed. If in sync, the INV SYNC LED indicates whether data is inverted or not as in AUTO.
SLAVE GATE	When on enables sync detection circuitry, bit counter, error counter and gated error out signal.
SLAVE RESET	When depressed the error and bit counts are set to zero.
TTL	When lit selects TTL or differential TTL interface as determined by rear panel switch TTL/DIFF.
ECL	Selects differential ECL interface when lit.
REMOTE	When lit indicates FLERT is in remote control mode and all other front panel funcions are disabled. Depressing the button will return FLERT to local. The FLERT cannot be put in remote mode via the front panel.

ERROR COUNT	When lit display shows current error count.
ERROR RATE	When lit display shows current error rate.
BIT COUNT	When lit display shows current bit count.
FREQ	When lit display shows current output frequency of internal synthesizer. The frequency may be changed by depressing the 3 buttons directly below the alphanumeric display.
DECR	When lit, depressing any of the buttons below the alphanumeric display will decrement the two digits directly above them if FREQ is also lit.

Section 5

System Description

FLERT II is constructed inside LINKABIT's universal chassis and has five internal modules:

1. Power Supplies - Provide +5V (TTL), -5.2V (ECL) and +24V (Syntest). Additional voltages are generated as necessary by on-board regulators from the main supplies.

2. Slave Board - (top board) Exclusively ECL circuitry for the slave generator, sync circuitry and error detect.

3. Master Board - This board is a combination ECL and TTL circuitry. Besides providing the master functions of clocking and pattern generation, this board has all the buffers and tranceivers for itself as well as the slave board for interfacing to the processor board and to the outside world.

4. Processor Board - This board contains the processor memory, SIO and GPIB interface circuitry, front panel controls and bit and error counters.

5. Syntest Board - (bottom board) Provides output frequency from 1 Mz to 15.99 MHz, programmable from the front panel. Additionally, some interface drivers and receivers are located on that board.

Hooking up the FLERT in a system is a straight forward task and is illustrated in Figure 5.1. Clock source to drive the master and/or the data source may be derived from an external source or from the FLERT internal synthesizer. The desired pattern may be selected from the front panel.

On the slave side, clock edge and sync mode may be slected as desired. To start or stop bit and error count, use the gate button. To clear the counters, use the reset button.

Various operating modes may be selected from the two dip switches located on the processor board. These are described in Section 6.

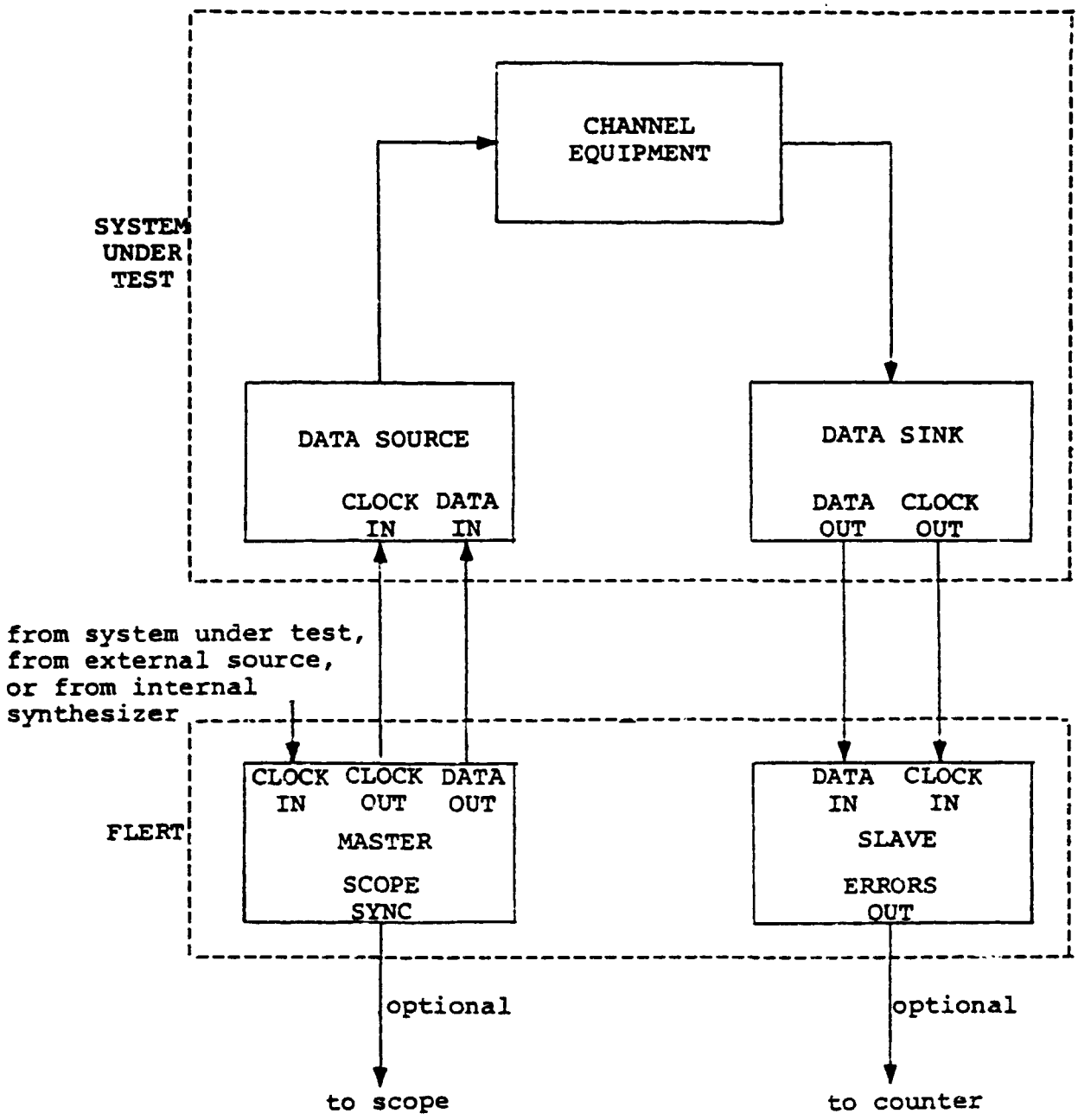


Figure 5.1. System Hook-Up

Section 6

Dip Switches

Two eight-position dip switches are located on the front of the processor board for selection of FLERT operating parameters in addition to the front panel. These switches are accesible by hinging open the front panel. The switch setting may be changed without turning power off or having to unplug the processor board.

The switch functions are detailed below.

SWITCH UP	ENABLE FRONT PANEL	FAST	GPIB	1 A4	1 A3	1 A2	1 A1	1 A0
SWITCH DOWN	DISABLE	SLOW	SIO	0	0	0	0	0
NORMAL MODE	UP	UP	UP	DN	UP	UP	UP	UP

GPIB Dip Switch (left switch)

SWITCH UP	DIFF	RITHI	R4	SYNCRUN	1 SPD3	1 SPD2	1 SPD1	1 SPD0
SWITCH DOWN	TTL	RITLO	R3	SYNCHOLD	0	0	0	0
NORMAL MODE	UP	UP	DN	UP	X	X	X	X

SIO Dip Switch (right switch)

GPIB Switch (left switch):

A4-A0: These switches determine the device address for FLERT in the GPIB mode.

GPIB/SIO: This switch selects remote control mode from SIO (RS-232 Serial-I/O or from GPIB.

FAST/SLOW: This switch selects an operating mode for the bit and error counters. In the "fast" mode reading of bit and error counter by the processor is inhibited when a carry is rippled through the counters. This is done to avoid a false reading during multiple transitions of the counters' outputs. In the "slow" mode reading is continuously enabled.

FRONT PANEL ENABLE:
This switch allows disabling controls from the front panel. The only operations allowed in this mode are looking at frequency, bit count, error count and error rate. This function has been installed so that nobody will interfere with your long running test during your absence from the lab.

SIO Switch (right side)

SPD3-SPD0: These switches select the baud rate for the RS-232 remote control and are detailed in that section.

SYNCRUN/SYNCHOLD:
In the normal SYNCRUN position the slave sync is in normal mode. Putting the switch in the SYNCHOLD mode has a meaning only when the front panel control is in manual mode. When this is the case, a single loss of sync will cause the Sync LED to remain in the off position indefinitely. This is a very useful feature if you want to detect a sync loss in a system during your absence. An example is a system such as a decoder or modem which looses sync due to "bit slip". In manual mode this will cause the Sync LED to go off and no resyncing will be attempted but a further "bit slip" may cause FLERT to sync again and you will have missed the loss of sync event.

R4/R3: For some applications it is desirable to divide the master clock by 4 rather than by 3. This is done by pushing the usual divide-by-3 front panel button, but putting this switch in the R4 position.

RITLO/RITHI: Selects a high or low rate integration threshold for resynchronization. At a high RIT longer bursts of errors are required to cause resynchronization. As an example, in the low RIT a burst of 26 consecutive errors is the shortest burst that will cause resync. In the high RIT, a burst of 344 consecutive errors is the shortest burst that will cause resync.

TTL/DIFF: This switch has effect when TTL interface is selected from the front panel. In the TTL position standard TTL interface is selected from the front panel BNC's. In the DIFF position RS-422 differential TTL interface mut be used from the rear panel.

Section 7

Remote Control

Remote control can be made through either RS-232 interface or from a GPIB controller (but not both at the same time). FLERT is put into remote mode automatically from the remote control terminal. In order to return FLERT to local mode, the remote button must be pushed on the front panel, otherwise all front panel commands are ignored.

The left dip switch on the processor board must be used to select GPIB/Serial I/O operation and the GPIB address. The right dip switch on the processor board is used to select the SIO speed. Figure 7.1 below describes these settings. The switch settings may be changed on-line but not while typing in commands or receiving data remotely.

Speed	Setting
300	0000
600	0001
1200	0010
2400	0011
4800	0100
9600	0101
19200	0110
not allowed	0111 ↕ 1111

Figure 7.1. SIO Speed

Generally a one-to-one correspondence exits between the front panel commands and the remote commands. The table below describes briefly each command. Multiple commands can be entered on a single line, separated by any number of spaces or commas. Command lines are executed by sending carriage return or line feed. In the RS-232 mode characters are echoed to the screen and data or messages sent back automatically. In the GPIB mode no messages are sent and data must be read-in explicitly. Either lower case or upper case characters may be used interchangeably.

MASTER

P4	Data pattern 4
P8	Data pattern 8
P11	Data pattern 11
P15	Data pattern 15
P16	Data pattern 16
PZ	All zero pattern
PINV	Invert pattern
PNORM	Normal pattern
MC+	Clock positive edge
MC-	Clock negative edge.
MD1	Clock divide by 1
MD2	Clock divide by 2
MD3	Clock divide by 3
ERON	Error add on
EROF	Error add off

SLAVE

SC-	Clock negative edge
SC+	Clock positive edge
AUTO	Auto sync
MAN	Manual sync
SYNC	Resync, valid only in manual mode
SINV	Sync to inverted data, valid only in manual mode.
SNORM	Sync to normal data, valid only in manual mode
GTON	Gate on
GTOF	Gate off
RST	Reset counters

MONITOR

FREQ	Display frequency
BTCT	Display bit count
ERCT	Display error count
ERRT	Display error rate

FREQUENCY

SETF	{X.XXX / XX.XX / XXX.X}	{Hz / KHz / MHz}	All digits must be entered including a decimal point

DATA

RFREQ	Read frequency
RBTCT	Read bit count
RERCT	Read error count
RERRT	Read error rate

STATUS

RSA	Read status ASCII. Data returned is identical to the command language and describes the complete state of the front panel buttons and LEDs.
RSB	Read status binary. Data returned is a bit map of the front panel state according to the following diagram.

	MSB	B6	B5	B4	B3	B2	B1	LSB
Byte 1 (first byte)	X	INV	GATE	INV SYNC	SET1	$2^{11}-1$	M+2	SCLK-
Byte 2	X	ALL ZEROS	M+3	SYNC	SET2	$2^{8}-1$	MCLK-	SCLK+
Byte 3	X	$2^{16}-1$	ERROR ADD	MANUAL	SET3	$2^{4}-1$	MCLK+	RESET
Byte 4 (last byte)	X	$2^{15}-1$	M+1	AUTO	DECR	REMOTE	ECL	TTL

Figure 7.2. ASCII Status Bytes

INTERFACE

ECL	ECL interface
TTL	TTL interface

GENERAL

INIT Returns FLERT to he following power-up state:

P16
PNORM
MC+
MD1
EROF
SC+
AUTO
GTOF
TTL
1.000 KHz frequency
BTCT
RST

MISCELLANEOUS

<DEL>	Deletes the current character (only in SIO)
<ESC>	Aborts the current command line or output stream (only in SIO)

Programming examples:

```
SIO:   ECL,GTON,P8,RST,BTCT <CR><LF>
       SETF 1.234 MHZ <CR><LF>
       RFREQ RBTCT RERCT RERRT RSA <CR><LF>

GPIB:  wrt 715,"ECL,GTON,P8,RST,BTCT" <EXECUTE>
       wrt 715,"SETF 1.234 MHZ" <EXLCUTE>
       wrt 715,"RFREQ RBTCT RERCT RERRT RSA" <EXECUTE>
       dim A$[100],B$[100],C$[100],D$[100],E$[100] <EXECUTE>
       red 715,A$,B$,C$,D$,E$, <EXECUTE>
```

Programming hint:

The RSA command returns an 11 (eleven) word string, each word of which is 7 characters long with at least two spaces for the last characters. The following lines may be added (following) the commands above) to start each word at a new line.

```
1 -> I
"loop": prt E$[I,I+6]
I+7 -> I
if I<78 go to "loop"
end
```

ACCEPTANCE TEST PROCEDURE

AND

TEST RESULTS

APPENDIX D

LINKABIT
CORPORATION
10453 ROSELLE ST. SAN DIEGO, CA. 92121
CODE IDENT NO. 11627

DOCUMENT NO. ATP 21370 REV. A

DATE 30 March 1981

ACCEPTANCE TEST PROCEDURE

FOR

DECODING SIMULATION SYSTEM

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REVISIONS

REV	DESCRIPTION	DATE	APPROVED
—	ORIGINAL RELEASE		
A	DCR 13278, DCR 14330	3/30/81	

1. INTRODUCTION

1.1 Purpose

The purpose of this procedure is to describe the tests to be performed at LINKABIT facilities on the simulation system for the convolutional encoded and symbol interleaved TDRSS S-Band return link service in a pulsed RFI environment.

2. APPLICABLE DOCUMENTS

The following document forms a part of this procedure to the extent specified herein. In the event of a conflict between this test procedure and the reference specification, the reference specification shall govern:

RFP #5-41508/187	Statement of Work for Development of a Simulation System for Validating the Analytical Prediction of Performance of the Convolutional Encoded and Symbol Interleaved TDRSS S-Band Return Link Service in a Pulsed RFI Environment

3. TEST REQUIREMENTS

3.1 General

The test item consists of the Simulation System, including the encoder/interleaver/deinterleaver/Viterbi decoder and the Transition Probability Generator (TPG).

The test philosophy is to use a Logic Analyzer to verify correct operation of the Transition Probability Generator and the encoder/interleaver, and then to use the Fast LINKABIT Error Rate Tester (FLERT) to verify proper operation (in terms of BER) of the decoder/deinterleaver.

This ATP will verify proper operation of the Simulation System at various levels of Gaussian noise. It will also verify synchronization times for the decoder and integrated decoder/deinterleaver, as well as specifying numerous other tests described below. Verification of these tests will imply compliance to all specifications cited in RFP #5-41508/187.

3.1.1 Description of Test Item. The unit under test is an integrated convolutional coding/symbol interleaving and integrated symbol deinterleaving/Viterbi decoding simulation system to be used to validate the analytically predicted performance of the TDRSS S-band return link with BPSK modulation in a pulsed RFI environment. Coding is either rate 1/2 or reduced metric rate 1/3. A transition probability generator converts a coded symbol bit to a 3 bit word based on a distribution loaded into the generator prior to the test. These 3 bit words are used to emulate the soft decision output of a BPSK demodulator and are subsequently Viterbi decoded.

3.2 Types of Tests

Three types of tests will be performed. The first group of tests will verify proper operation of the encoder, interleaver, and TPG using an HP1610A Logic Analyzer. Once performance of these is verified, the deinterleaver/decoder operation will be tested by means of a bit error rate test. The third type of test will test synchronization time. Synchronization time will be defined as the number of bit times from the occurrence of an event that leads to loss of sync to the point at which the deinterleaver/decoder achieves the correct sync state. Errors due to the loss of sync may be produced after the unit achieves proper sync, but these cannot be distinguished from noise induced errors. Occurrence of such errors will cease within 3600 bit times after the deinterleaver achieves proper sync due to the nature of the design.

In addition to these three types of tests, LINKABIT will conduct a system test using government furnished data. Failure to meet performance predicted analytically by the government for these tests shall in no way be construed as failure of the unit under test.

3.3 Test Control

Tests are to be performed under the supervision of LINKABIT engineering. LINKABIT engineering is to maintain a log of events.

The Contracting Officer is to be notified sufficiently in advance of testing to allow his representative to witness and verify each test.

All data taken during in-plant testing is to be properly identified and retained for incorporation in the Test Report. The Test Engineer will be responsible for recording all pertinent data, including the following:

a. Results of tests
b. Date of test
c. Signature of Test Engineer and Witness
d. Test conditions as required
e. List of Test Equipment (Mfr., Model, Ser. Nos., and calibration due date).

4. TEST EQUIPMENT

4.1 Test Equipment Required

The following test equipment is required:

HP1610A Logic Analyzer
ATP Data Cassettes #1 and #2
LV7017 extender card
LV7017 cables
BNC cables.

4.2 Test Setup

Connect the test equipment as shown in figure 1.

4.3 Initial Control Positions

Power up all devices.

4.3.1 FLERT Setup. Refer to FLERT manual for operating instructions.

a. CONTROL TTL
b. MONITOR FREQUENCY = 6 MHz
c. MASTER CLOCK+, ÷2, ALL ZEROES, ERROR-ADD OFF
d. SLAVE CLOCK-, AUTO

4.3.2 Calcualtor Setup.

a. Insert program cassette
b. Load special function keys (ldk 1, execute). Depress "RESET" (f5)
c. Load LOADTEST program (s/f key f8)
d. Insert ATP data cassette #1.

4.3.3 TPG Setup. The BYPASS, BITSLIP, and INVERT switches should be in "normal" position.

4.3.4 LV7017 Setup. Place the LV7017 in serial mode, on line with the interleaver out. Set the dipswitches as follows:

1 : ON (encoder generators not reversed)
2 : ON (differential encoding off)
3 : ON (encoder alternate symbols not inverted)
4 : OFF (decoder alternate symbols not inverted)
5 : ON (differential decoding off)
6 : ON (rate 1/2)
7 : ON (shorter path memory)
8 : OFF (decoder generators not reversed)

NOTE

"ON" means ON-side is depressed.
"OFF" means OFF-side is depressed.

4.3.5 Cable Connections. Cable connections are via TWINAX BNCs; FLERT connections to rear panel differential connectors.

a. Connect FLERT INT CLK to LV7017 ENC 2R CLK IN
b. Connect LV7017 ENC 2R CLK to FLERT MASTER CLK IN
c. Connect FLERT DATA OUT to LV7017 ENC DATA IN
d. Connect FLERT SLAVE CLK IN to LV7017 DEC R CLK
e. Connect FLERT DATA IN to LV7017 DEC DATA OUT.

5. TEST PROCEDURE

5.1 Output and State Distributions of "Transition Probability Generator" (TPG)

This test uses the HP1610A Logic Analyzer to verify the operation of the TPG by counting the occurrences of each output and state and manually comparing them to the input data.

5.1.1 Test Equipment Setup.

a. FLERT. Set up as in 4.3.1.
b. LV7017. Set up as in 4.3.4.
c. TPG. Set up as in 4.3.3.
d. Logic Analyzer. Set up as follows:

1. Format specification:

CLOCK: [+]

	—POD 4—	PODS 3,2,1
LABEL ASSIGNMENT:	BBBBBAAA	XXXXXXXX

	A	B
POLARITY:	[+]	[+]
NUM. BASE:	[BIN]	[BIN]

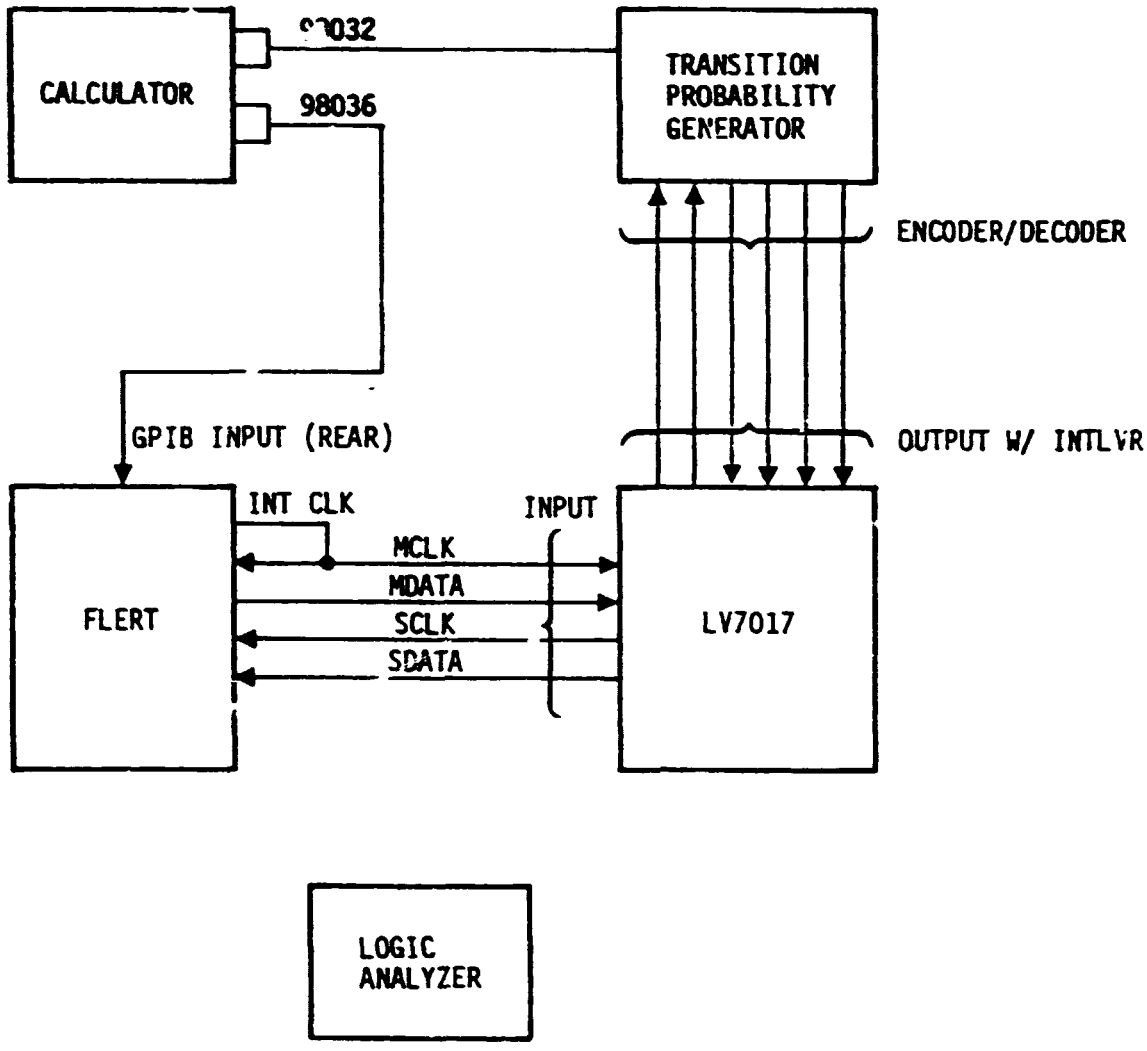

Figure 1. Test Setup

1788

2. TRACE specification:

   [START] TRACE XXX XXXXX

   TRACE [ONLY] XXX XXXXX 02000

   COUNT [STATES] 011 XXXXX

3. LIST specification:

   STATE COUNT [ABS]

4. Connect PODs to TPG board as follows:

   CLOCK: CLK U202-9
          GND U202-8

POD4:	BIT 7	U605-3	B field:	distribution state
	6	U604-6		
	5	U604-5		
	4	U604-4		
	3	U604-3		
	2	U202-11	A field:	quantized output symbols
	1	U202-6		
	0	U202-4		
	GND	U605-8		

5. Calculator. Run LOADTEST Program. Load track 0, file 3 from ATP data cassette #1. When load is complete, depress START (s/f key f2).

5.1.2 Output Distribution. The Logic Analyzer will trace every 2000 clocks for a total of 126,000, and counts every occurrence of the output selected in the "count states" field of the trace specification. The total count appears in the STATE COUNT column of line +63.

a. Perform a trace. The STATE COUNT at line +63 is the number of occurrences of output 011 in any state in 126,000 clocks. Record the result on the data sheet.

b. Change the TRACE specification to the following:

   COUNT [STATE] 010 XXXXX

   Perform a trace. Record the count at line +63 on the data sheet.

c. Repeat for COUNT [STATES]

1. 001 XXXXX
2. 000 XXXXX
3. 100 XXXXX
4. 101 XXXXX
5. 110 XXXXX
6. 111 XXXXX

Record the counts at line +63 on the data sheet.

d. Compare the observed results to the expected values. Results should agree with expected values to within 20%. Due to the probabilistic nature of these results, failure to agree will not be construed as a test failure.

5.1.3 State Distribution. The state distributions will be verified in the same manner as the output distribution.

a. Change the TRACE specification to the following:

COUNT [STATES] XXX 00000

Perform a trace. The STATE COUNT at line +63 is the number of occurrences of any output in state 00000 in 126,000 clocks. Record this count on the data sheet.

b. Change the TRACE specification to the following:

COUNT [STATES] XXX 00001

Perform a trace. Record the count at line +63 on the data sheet.

c. Repeat for states XXX 00010
XXX 00011
XXX 00100

Record the counts on the data sheet.

d. Compare the observed results to the expected values. Results should agree to within 20%. Failure to agree will not be construed as a test failure.

5.1.4 Hold States. Reset the TPG (s/f key f5). Run LOADTEST and load track 0 file 6. When load is complete depress START (s/f key f2). Change the Logic Analyzer TRACE specification as follows:

```
[START]  TRACE    XXX 00000
TRACE    [ALL]
COUNT    [OFF]
```

a. Perform a trace. The Logic Analyzer will trigger when the TPG reaches state 00000. This state has a hold time of 0, thus a new state should appear at line +01. (The value of field A is irrelevant.) Record the result (P/F) on the data sheet.

b. Insert a trigger qualifier in the TRACE specification.
Set FIND IN SEQUENCE XXX 00000
Set [START] TRACE XXX 00001

Perform a trace. The logic analyzer will trigger on reaching state 00001. A new state should appear at line +11. Record the result (P/F) on the data sheet.

c. Set [START] TRACE XXX 00010 and perform a trace. A new state should appear at line +21.
Repeat for states XXX 00011 (new state at +31)
XXX 00100 (new state at +41)
Record the results (P/F) on the data sheet.

5.2 Encoder Operation

This test uses the HP1610A Logic Analyzer to verify proper encoder operation.

5.2.1 Test Equipment Setup.

a. FLERT. Set up FLERT as in 4.3.1, except place MASTER ERROR-ADD to ON.

b. LV7017. Set up LV7017 as in 4.3.4. Place the I/O board on the extender card.

c. TPG. The TPG is not used in this test.

d. Logic Analyzer. Set up the HP1610A Logic Analyzer as follows:

1. FORMAT specification:

```
CLOCK:  [+]

LABEL          ——— POD 4 ———      —— PODS 3,2,1 ——
ASSIGNMENT:  X X X X X X A A      X X X X X X X X

POLARITY:  [+]

NUM. BASE:  [BIN]
```

2. TRACE specification:

   [START] TRACE 1X

   TRACE [ALL STATES]

   COUNT [OFF]

3. Connect pods to I/O board as follows:

CLOCK:	CLK	U107-3	symbol clock
	GND	U107-7	ground
POD4:	BIT 1	U103-4	data in
	BIT 0	U107-5	data out
	GND	U103-8	ground

5.2.2 Procedure.

a. The encoder mode switches are set to rate 1/2, G1, and G2 normal mode. Perform a trace. The resulting trace should be as shown on the data sheet. Record the result (P/F) on the data sheet.

b. Set the encoder mode switches to rate 1/2, with G1 and G2 reversed as follows:

   1. OFF (generators reversed)
   2. ON (differential encoding off)
   3. ON (alternate symbols not inverted)
   6. ON (rate 1/2)

   Perform a trace. The resulting trace should be as shown on the data sheet. Record the result (P/F) on the data sheet.

c. Set the encoder mode switches to rate 1/2, with alternate symbols inverted as follows:

   1. ON (generators not reversed)
   2. ON (differential encoding off)
   3. OFF (alternate symbols inverted)
   6. ON (rate 1/2)

   Perform a trace. The resulting trace should be as shown on the data sheet. Record the result (P/F) on the data sheet.

d. Set the encoder mode switches to rate 1/3, normal mode as follows:

1. ON (generators not reversed)
2. ON (differential encoding off)
3. ON (alternate symbols not inverted)
6. OFF (rate 1/3)

Change the FLERT Master Clock divider to ÷3. Perform a trace. The resulting trace should be as shown on the data sheet. Record the result (P/F) on the data sheet.

e. Set the encoder mode switches to rate 1/3, alternate symbols inverted as follows:

1. ON (generators not reversed)
2. ON (differential encoding off)
3. OFF (alternate symbols inverted)
6. OFF (rate 1/3)

Perform a trace. The result should be as shown on the data sheet. Record the result (P/F) on the data sheet.

5.3 Decoder Operation

The following group of tests demonstrates proper functioning of the Viterbi decoder in all its modes. The tests involve measuring BER at various levels of E_b/N_o. The decoder shall be determined to be operating correctly if it produces the expected bit error rate in AWGN provided by the TPG. Due to the probabilistic nature of BER tests, failure of the decoder to produce the exact BER expected cannot be construed as a test failure. BER should fall between the minimum and maximum values listed on the data sheet.

5.3.1 Test Equipment Setup.

a. FLERT. Setup as in 4.3.1, except: PATTERN = $2^{16}-1$.

b. LV7017. Setup as in 4.3.4.

c. Logic Analyzer. The Logic Analyzer is not used in this test.

d. TPG. Setup as in 4.3.3.

5.3.2 E_b/N_o 4.4 dB, Rate 1/2 Decoding. For this test, it will be determined that the LV7017 can successfully decode in all rate 1/2 configurations at an E_b/N_o of 4.4 dB.

a. Reset TPG (s/f key f5). Run LOADTEST and load track, 0 file 6 from ATP data cassette #2. Depress START (s/f key f2).

b. Turn FLERT Gate ON. The LV7017 dipswitches have been set for rate 1/2 normal mode.

c. Reset FLERT and observe ERROR RATE for 2 minutes. Bit error rate should be 10^{-5}. Record result on the data sheet.

d. Change LV7017 dipswitches as follows:

1. OFF (generators reversed)
8. ON

e. Reset FLERT. Observe ERROR RATE for 2 minutes. Bit error rate should be 10^{-5}. Record result on the data sheet.

f. Change LV7017 dipswitches as follows:

1. ON (encoder generators not reversed)
3. OFF (alternate encoder symbols inverted)
4. ON (alternate decoder symbols inverted)
8. OFF (decoder generators not reversed)

g. Reset FLERT. Observe ERROR RATE for 2 minutes. Bit error rate should be 10^{-5}. Record result on the data sheet.

5.3.3 Rate 1/2 Decoder Output Error Rates. For this test, it will be determined that the decoder produces the expected output error rate in rate 1/2 normal mode at E_b/N_o of 3.0, 3.75 and 5.1 dB.

a. Return LV7017 dipswitches to positions established in 4.3.4 (rate 1/2, normal).

b. Run LOADTEST and load track 0 file 12 from ATP data cassette #1. Depress START (s/f key f2). Reset FLERT and observe ERROR RATE for 2 minutes. BER should be $9X10^{-4}$. Record result on the data sheet.

c. Run LOADTEST and load track 0 file 18 from ATP data cassette #1. Depress START (s/f key f2). Reset FLERT

and observe ERROR RATE for 2 minutes. BER should be 10^{-4}. Record result on the data sheet.

d. Run LOADTEST and load track 0 file 24 from ATP data cassette #1. Depress START (s/f key f2). Reset FLERT and observe ERROR RATE for 5 minutes. BER should be 10^{-6}. Record result on the data sheet.

5.3.4 E_b/N_o = 4.1 dB, Rate 1/3 BER. For this test, it will be determined that the decoder produces the expected BER at both rate 1/3 configurations at an E_b/N_o of 4.1 dB.

a. Change LV7017 dipswitches as follows:
6. OFF (rate 1/3 normal)
Change FLERT Master Clock divider to ÷3. Run LOADTEST and load track 1, file 0 from ATP data cassette #1. Depress START (s/f key f2).

b. Reset FLERT. Observe ERROR RATE for 2 minutes. BER should be 10^{-5}. Record result on the data sheet.

c. Change LV7017 dipswitches as follows:
3. OFF (rate 1/3, alternate symbols
4. ON inverted)
Reset FLERT. Observe ERROR RATE for 2 minutes. BER should be 10-5. Record result on the data sheet.

5.3.5 E_b/N_o = Various, Rate 1/3 BER. For this test, it will be determined that the decoder produces the expected BER in rate 1/3 normal mode at E_b/N_o of 2.5, 3.4, and 4.8 dB.

a. Change LV7017 dipswitches as follows:
3. ON (rate 1/3 normal)
4. OFF

b. Run LOADTEST and load track 1, file 6 from ATP data cassette #1. Depress START (s/f key f2). Reset FLERT and observe ERROR RATE for 2 minutes. BER should be 10^{-3}. Record result on the data sheet.

c. Run LOADTEST and load track 1, file 12 from ATP data cassette #1. Depress START (s/f key f2). Reset FLERT and observe ERROR RATE for 2 minutes. BER should be 10^{-4}. Record result on the data sheet.

d. Run LOADTEST and load track 1, file 18 from ATP data cassette #1. Depress START (s/f key f2). Reset FLERT and observe ERROR RATE for 5 minutes. BER should be 10^{-6}. Record result on the data sheet.

5.4 Interleaver Operation

This test will verify the interleaver PN sequence, and verify that the symbol from the encoder G1 generator is covered by the first bit of the PN sequence and that it enters the top tap (zero-delay) path of the interleaver.

5.4.1 Test Equipment Setup.

a. FLERT. Set up FLERT as in 4.3.1.

b. LV7017. Set up LV7017 as in 4.3.4. Place interleaver board on the extender card. Switch INTERLEAVER IN.

c. TPG. The TPG is not used in this test.

d. Logic Analyzer.

1. FORMAT specification:

CLOCK: [+]

	—POD 4—	—POD 3—	PODS 2,1
LABEL ASSIGNMENT:	AAA BBBBB	XXX CCCCC	XXXXXXXX

	A	B	C
POLARITY:	[+]	[+]	[+]
NUM. BASE:	[BIN]	[DEC]	[DEC]

2. TRACE specification:

[START] TRACE 1XX XXX XXX

TRACE [ALL]

COUNT [OFF]

3. Connect PODs to interleaver board as follows:

CLOCK:	CLK	U206-1	ICLOCK
	GND	U206-8	
POD4:	BIT 7	U003-15	Start PN
	6	U303-6	Rate Clock
	5	U303-12	PN sequence
	4	U206-13	WRITE address
	3	U205-3	
	2	U205-6	
	1	U205-10	
	0	U205-13	
	GND	U206-8	

POD3:	BIT 4	U206-14	READ address
	3	U205-2	
	2	U205-5	
	1	U205-11	
	0	U205-14	
	GND	U205-8	

5.4.2 PN Sequence. Perform a trace. The listing on the Logic Analyzer should appear as on the data sheet. The PN sequence appears in the third column of the A field, with the first bit of the sequence in line +01. The B and C fields are irrelevant. Record result (P/F) on the data sheet.

5.4.3 PN and Tap Synchronization.

a. Perform a trace. Line +01 of the listing represents the "top tap" (zero delay). This line should appear as follows: +01 010 N N

(Where N can be any number from 02 to 31 inclusive.) This result shows the rate clock high, the first bit of the PN sequence and that the write address is the same as the read address. Repeat 4 times and record the result (P/F) on the data sheet.

b. Set [START] TRACE 101 31 31. Perform a trace. The Logic Analyzer display should appear as on the data sheet. Record result (P/F) on the data sheet.

c. Set FLERT Master Clock divider to ÷3. Set LV7017 dip-switch 6 to rate 1/3 (OFF). Perform a trace. The Logic Analyzer display should appear as on the data sheet. Record result (P/F) on the data sheet.

5.5 Deinterleaver Operation

The deinterleaver will be tested in two different ways. The first test will verify that a burst of 30 bits is dispersed so that 120 bit times or more separate each pair of bits in the burst in the deinterleaved sequence. The second test will verify that the BER of the combined CODEC and interleaver/deinterleaver is the expected value for both rate 1/2 and rate 1/3 in the presence of Gaussian noise.

5.5.1 Test Equipment Setup.

a. FLERT. Set up as in 4.3.1, except: PATTERN INVERT = ON.

b. LV7017B. Set up as described in 4.3.4. Place interleaver on extender card. Remove DROM V103 on interleaver and replace with test PROM 1, an unprogrammed (i.e. all addresse=0) PROM.

c. TPG. Reset TPG (s/f key f5). Run loadtest and load from ATP test tape #2 file 0, track 0. Depress START (f2).

d. Logic Analyzer.

1. FORMAT specification:

CLOCK: [+]

LABEL ASSIGNMENT:	-POD 4- XXXXXXX	PODS 3.2.1 XXXXXXXX

A
POLARITY: [+]

NUM. BASE: [HEX]

2. Trace Specification

[START] TRACE 0

TRACE [ONLY STATES] 0

COUNT [STATES] X

3. Connect PODS to interleaver card as follows:

CLOCK:	CLK	A103-9	CLOCK
	GND	A103-8	
POD 4:	BIT 0	A104-10	SIGN BIT out of deinterleaver prior to PN ADD.
	GND	A104-7	

5.5.2 Deinterleaver Burst Dispersion Capability.

Perform a trace. The output of the encoder/interleaver is an all one's data stream. The TPG contains two states. The higher probability state is a perfect channel state in which no errors are introduced. The lower probability state is a length 30 burst during which all channel symbols are inverted. If the deinter-

leaver is performing properly, these symbols will be separated from each other by at least 119 bits. Verify that this is so by observing that the relative state count displayed on the logic analyzer trace is at least 119 for each state. Record the result (P/F) on the test data sheet.

5.5.3 Test Equipment Setup.

a. FLERT. Set up FLERT as in 4.3.1, except: PATTERN = $2^{16}-1$.

b. LV7017. Set up LV7017 as in 4.3.4. Remove test PROM #1 from the location of V103 and replace PROM V103 on the interleaver card. Place interleaver back into chassis. Switch INTERLEAVER IN.

c. TPG. Reset TPG (s/f key f5). Run LOADTEST and load track 0, file 6 from ATP cassette #2. Depress START (f2).

d. Logic Analyzer. The Logic Analyzer is not used in this test.

5.5.4 Rate 1/2 Normal. Reset FLERT and observe ERROR RATE for 2 minutes. BER should fall in the range shown on the data sheet. Record result on the data sheet.

5.5.5 Rate 1/3 Normal. Set LV7017 dipswitch 6 to rate 1/3 (OFF). Set FLERT Master Clock divider to -3. Run LOADTEST and load track 1, file 0. Reset FLERT and observe ERROR RATE for 2 minutes. BER should fall in the range shown on the data sheet. Record result on the data sheet.

5.6 Initial Synchronization

The TPG contains a distribution of 5 states such that the first four produce 50% channel errors but have quality bits fitting a Gaussian distribution of E_b/N_o 4.4 dB, and the fifth is 4.4 dB at rate 1/2. The transition probabilities are such that the TPG will progress from state 1 to state 5 in about 40 seconds.

5.6.1 Test Equipment Setup.

a. FLERT. Set up FLERT as in 4.3.1, except: PATTERN = $2^{16}-1$.

b. LV7017. Set up LV7017 as in 4.3.4, except: place the I/O board on an extender card and switch INTERLEAVER IN.

c. Logic Analyzer.

1. FORMAT specification:

CLOCK: [+]

LABEL	——4——	——3——
ASSIGNMENT:	XBBAAAAA	XXXXXXXC

	A	B	C
POLARITY:	[+]	[+]	[+]

NUM. BASE: [HEX] [BIN] [BIN

2. TRACE specification:

[START] TRACE 04 XX X

TRACE [ONLY] XX XX X 03000

COUNT [STATE] XX XX 1

3. LIST specification:

STATE COUNT [REL]

4. Connect the pods to the I/O board and TPG board as follows:

CLOCK:		U804-2	RCLK	(I/O board)
POD4:	BIT 6	U000-3	BITSLIP	(TPG board)
	5	U000-6	INVERT	
	4	U605-3		
	3	U604-6		
	2	U604-5	"state"	
	1	U604-4		
	0	U604-3		
POD3:	BIT 0	U804-10	SYNCLOSS	(I/O board)

d. Reset TPG (s/f key f5). Run LOADTEST. Load track 1 file 24 from ATP data cassette #1.

5.6.2 Performance Test. Perform a trace. Depress START (f2). When the TPG reaches the Gaussian noise state, the logic analyzer will trigger. It will trace every 3000 clocks and count the SYNCLOSS signals. The initial synchronization time is the number of clocks between the trigger and the last SYNCLOSS. The last SYNCLOSS occurs in the last line in which a non-zero count

appears in the STATE COUNT column. The number of clocks is this line number multiplied by 3000. Record this result on the data sheet.

5.6.3 To repeat this test, depress STOP (s/f key f4) and repeat paragraph 5.6.2. Repeat 9 times and record the results on the data sheet.

5.7 Resynchronization

This test will verify the resynchronization time after a bitslip or a phase inversion both with and without the interleaver.

5.7.1 Test Equipment Setup.

a. FLERT. Set up FLERT as in 4.3.1, except: PATTERN = $2^{16}-1$.

b. LV7017. Set up LV7017 as in 4.3.4, except: place the I/O board on an extender card and switch INTERLEAVER OUT.

c. Logic Analyzer.

1. FORMAT specification:

CLOCK: [+]

LABEL	4	3
ASSIGNMENT:	XBBAAAAA	XXXXXXXC

	A	B	C
POLARITY:	[+]	[+]	[+]

NUM. BASE: [HEX] [BIN] [BIN]

2. TRACE specification:

[START] TRACE XX 0X X

TRACE [ONLY] XX XX X 00100

COUNT [STATES] XX XX 1

3. LIST specifications:

STATE COUNT [REL]

4. PODS:

CLOCK:		U804-2	RCLK	(I/O board)
POD4:	BIT 6	U000-3	BITSLIP	(TPG board)
	5	U000-6	INVERT	
	4	U605-3		
	3	U604-6		
	2	U604-5	"state"	
	1	U604-4		
	0	U604-3		
POD3:	BIT 0	U804-10	SYNCLOSS	(I/O board)

d. TPG. Place BITSLIP, INVERT, and BYPASS switches in NORMAL position. Reset TPG (s/f key f5). Run LOAD-TEST and load track 0, file 0 from ATP data cassette #1. Depress START (s/f key f2).

5.7.2 Procedure.

a. Perform a trace. Switch BITSLIP from NORMAL to DELAYED. The BITSLIP switch will trigger the logic analyzer. The resynchronization time after introduction of one clock delay is the number of clocks between the trigger and the last SYNCLOSS. The number of clocks is the number of the last line containing a non-zero state count multiplied by 100. It should be less than 500. Record this result on the data sheet. Set BITSLIP switch to normal.

b. Repeat 4 times, recording results on the data sheet.

c. Change TRACE specification on Logic Analyzer to: [START] TRACE XX X0 X. Return BITSLIP switch to normal. Perform a trace. Switch INVERT. This will trigger the Logic Analyzer. The resynchronization time after an inversion is the number of clocks between the trigger and the last appearance of SYNCLOSS. Record this result on the data sheet.

d. Repeat 4 times, recording results on the data sheet.

e. Return INVERT switch to NORMAL. On the LV7017, switch INTERLEAVER IN. On the Logic Analyzer, change TRACE specification to:
[START] TRACE XX 0X X
TRACE [ONLY] XX XX X 01000

Perform a trace. Switch BITSLIP from NORMAL to DELAYED. The resynchronization time is the number of clocks between the trigger and the last appearance of

SYNCLOSS. This number is the number of the last line containing a nonzero state count multiplied by 1000. Record this result on the data sheet. Set switch to NORMAL. Repeat 3 times.

f. Change logic analyzer trace specification to the following:
[START] TRACE XX 1X X
TRACE [ONLY] XX XX X 01000

Set BITSLIP switch to delayed. Perform a trace. Throw switch to NORMAL. Record synchronization time as described in the previous paragraph on the data sheet. Repeat 3 times.

6. TEST OF AUTOMATED TEST PROGRAM

Setup the LV7017 as in INITIAL SETUP. Insert program cassette and load program RUNTEST (s/f key f11). Verify that the HP9825 is connected to the FLERT via HPIB interface and that the select code of the interface is set to 7. Depress "RUN" on the HP9825.

The HP9825 will request a variety of information. Enter the following data.

Number of tests: 3
Rate: 1/2
track#: 0
file#: 12
symbol clock: 6000000
Pattern: 15
inverted pattern: no (s/f key 1)
length of test: 3.6e8
track#: 0
file#: 18
symbol clock: 4000000
Pattern: 11
inverted pattern: yes (s/f key 0)
length of test 4.0e8
track#: 0
file#: 0
symbol clock: 6000000
Pattern: 16
inverted pattern: no (s/f key 1)
length of test: 5.0e8

Depress CONTINUE. The HP9825 will setup and start test #1 which will run until the FLERT has recorded more than $3.6X10^8$ bits. For the duration of test #1 the FLERT should display error rate,

pattern 2^{15}-1, Master clock ÷2 and pattern invert off. The HP9825 will record the error rate on its paper printout at the conclusion of the test. This should be between $7X10^{-4}$ and $1.1X10^{-3}$. Record the result (Pass/Fail) on the data sheet.

For test #2 the FLERT should display error rate, pattern 2^{11}-1, pattern invert on, and Master clock ÷2. The error rate recorded at the conclusion of the test should be between $8X10^{-5}$ and $1.2X10^{-4}$. Record the result (Pass/fail) on the data sheet.

For test #3 the FLERT should display error rate, pattern 2^{16}-1, pattern invert off, and Master clock ÷2. The error rate recorded at the conclusion of the test should be between $8X10^{-6}$ and $1.2X10^{-5}$. Record the result (Pass/fail) on the data sheet.

7. GOVERNMENT DATA TESTS

Prepare a data tape on the HP9825 for the specified distribution (see TPG manual). Run the LOADTEST program to load the distribution into the TPG. Set up the FLERT and LV7017 as needed for the test. Depress START (s/f key f2 on the HP9825). RESET the FLERT. Record the results of the test and the type of test on the data sheet.

APPENDIX A

ATP DATA TAPE #1

trk	file	
0	0	5 identical distributions of E_b/N_o = 4.4 dB at rate 1/2. State transitions are independent of state. No hold.
0	6	5 identical no noise distributions. Equal state probabilities. Varying hold times.
0	12	1 state : rate 1/2 E_b/N_o 3.0 dB
0	18	1 state : rate 1/2 E_b/N_o 3.75 dB
0	24	1 state : rate 1/2 E_b/N_o 5.1 dB
1	0	1 state : rate 1/3 E_b/N_o 4.1 dB
1	6	1 state : rate 1/3 E_b/N_o 2.5 dB
1	12	1 state : rate 1/3 E_b/N_o 3.4 dB
1	18	1 state : rate 1/3 E_b/N_o 4.8 dB
1	24	Initial synchronization test. 4 states of anarchy. 1 state of E_b/N_o 4.4 dB at rate 1/2.

trk 0/file 0

State	Prob
0	102
1	51
2	51
3	26
4	26

trk 0/file 6

State	Hold
0	0
1	10
2	20
3	30
4	40

ATP DATA TAPE #2

trk	file	
0	0	No errors: occasional bursts of 30 errors (2 states)
0	6	Rate 1/2 E_b/N_o = 4.4 dB 1 state Gaussian

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

Test Engineer Steven J. Zeuch NASA Representative Denver W. Herr
DENVER W. HERR

Date 3-5-81

HP1610A cal. date: Due 7-2-81

TEST 1: TPG Output and State Distributions

TEST	OUTPUT	RESULT EXPECTED	MIN	MAX	COUNT
Paragraph 5.1.2 Output distribution	011	71890	57512	86268	71023
	010	22733	18186	27280	22937
	001	16334	13067	19600	16346
	000	9167	7333	11000	9506
	100	4030	3224	4836	4136
	101	1384	1107	1660	1473
	110	369	295	443	438
	111	92	74	110	95
	State				
Paragraph 5.1.3 State distribution	00000	50203	40162	60244	50193
	00001	25102	20082	30122	25048
	00010	25102	20082	30122	24974
	00011	12797	10238	15356	12812
	00100	12797	10238	15356	12787
	Trigger on State	New state should appear at line #			Pass/Fail
Paragraph 5.1.4 Hold states	00000	+01			Pass
	00001	+11			Pass
	00010	+21			Pass
	00011	+31			Pass
	00100	+41			Pass

Acceptance Test Procedure Data Sheet for Decoding Simulation System

Test Engineer Steve M. Gardner NASA Representative Lewis V. Hicks DENVER W. II ERR

Date 3-5-81

TEST 2: Encoder Operation

Paragraph: / Test:	5.2.2a rate 1/2 normal	5.2.2b rate 1/2 generators reversed	5.2.2c rate 1/2 alternate symbols inverted	5.2.2d rate 1/3 normal	5.2.2e rate 1/3 alternate symbols inverted
START	10	10	10	10	10 or 11
+01	10	10	11	10	11 10
+02	00	00	00	10	10 11
+03	00	00	01	00	01 00
+04	01	01	01	00	00 01
+05	01	01	00	01	001 010
+06	01	00	01	01	010 001
+07	00	01	01	01	001 010
+08	01	01	01	01	010 001
+09	01	01	00	00	010 001
+10	01	01	01	01	010 001
+11	01	01	00	01	001 010
+12	00	00	00	01	010 001
+13	00	00	01	01	001 010
+14	00	01	00	01	010 001
+15	01	00	00	01	001 010
+16	01	01	01	00	001 010
+17	01	01	00	00	010 001
+18	00	00	00	00	001 010
+19	00	00	01	01	001 010
+20	00	00	00	00	001 010
+21	00	00	01	01	001 010
+22	00	00	00	00	001 010
+23	00	00	01	01	001 010
+24	00	00	00	01	010 001
+25	00	00	01	01	001 010
+26	00	00	00	00	~~00~~ ~~01~~
.					
.					
.					
Pass/Fail:	Pass	Pass	Pass	Pass GENERATOR COEFFICIENTS VERIFIED LWH	Pass

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

Test Engineer Steven J. Gurd NASA Representative Denver W. Herr
DENVER W. HERR

Date 3-5-81

TEST 3: Decoder Operation

TEST	RESULTS EXPECTED	MIN	MAX	Pass/Fail
Paragraph 5.3.2				
E_b/N_o = 4.4 dB, rate 1/2				
normal	10^{-5}	8×10^{-6}	1.2×10^{-5}	9.931×10^{-6} pass
generators reversed	10^{-5}	8×10^{-6}	1.2×10^{-5}	9.916×10^{-6} pass
alternate symbols inverted	10^{-5}	8×10^{-6}	1.2×10^{-5}	9.913×10^{-6} pass
Paragraph 5.3.3				
rate 1/2, normal				
E_b/N_o = 3.0 dB	9×10^{-4}	7×10^{-4}	1.1×10^{-3}	8.305×10^{-4} pass
3.75 dB	10^{-4}	8×10^{-5}	1.2×10^{-4}	9.802×10^{-5} pass
~~5.0~~ 5.1 dB	10^{-6}	8×10^{-7}	1.2×10^{-6}	1.194×10^{-6} pass
Paragraph 5.3.4				
rate 1/3,				
E_b/N_o = 4.1 dB				
normal	10^{-5}	8×10^{-6}	1.2×10^{-5}	1.100×10^{-5} pass
alternate symbols inverted	10^{-5}	8×10^{-6}	1.2×10^{-5}	1.094×10^{-5} pass
Paragraph 5.3.5				
rate 1/3, normal				
E_b/N_o = 2.5 dB	10^{-3}	8×10^{-4}	1.2×10^{-3}	1.105×10^{-3} pass
3.4 dB	10^{-4}	8×10^{-5}	1.2×10^{-4}	1.038×10^{-4} pass
~~4.7~~ 4.9 dB	10^{-6}	8×10^{-7}	1.2×10^{-6}	8.264×10^{-7} pass

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

Test Engineer Steven J. Hall NASA Representative Denver W. Herr
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Date 3-5-81

TEST 4: Interleaver Operation

TEST	LOGIC ANALYZER DISPLAY		PASS/FAIL
Paragraph 5.4.2 PN Sequence	START	101	PASS
	+01	010	
	+02	000	
	+03	010	
	+04	000	
	+05	010	
	+06	001	
	+07	011	
	+08	001	
	+09	010	
	+10	000	
	+11	011	
	+12	000	
	+13	010	
	+14	000	
	+15	011	
	+16	000	
	+17	011	
	+18	000	
	+19	011	
	+20	001	
	+21	011	
	+22	001	
	+23	010	
	+24	001	
	+25	011	
	+26	000	
	+27	011	
	+28	000	
	+29	010	
	+30	101	
	+31	010	
	+32	000	PASS
	.	.	
	.	.	
	.	.	

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

Test Engineer Steven K. Gee NASA Representative Denver W. Herr

Date 3-5-81

TEST 4: Interleaver Operation (Continued)

TEST	LOGIC ANALYZER DISPLAY	PASS/FAIL
Paragraph 5.4.3.a PN Synchronization	A B C START 101 N-1 N or N-1 +01 01C N N	Pass Pass
Paragraph 5.4.3.b Tap Synchronization rate 1/2	A B C START 101 31 31 +01 010 02 02 +02 000 03 02 +03 010 04 02 +04 000 05 02 +05 010 06 02 +06 001 07 02 +07 011 08 02	Pass Pass
Paragraph 5.4.3.c Tap Synchronization rate 1/3	A B C START 101 31 31 +01 010 02 02 +02 010 03 02 +03 000 04 02 +04 010 05 02 +05 010 06 02 +06 001 07 02 +07 011 08 02 +08 011 09 02	Pass Pass

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

ATP 21.3.0

Test Engineer Steve J. Gaud NASA Representative Lewis W. Hess
DENVER W. HESS

Date 3-5-81

TEST 5: Deinterleaver Operation

TEST	RESULTS EXPECTED	MIN	MAX	PASS/FAIL
Paragraph 5.5.2 Deinterleaver burst dispersion	~~State count=120 for each state~~ 119*			Pass
Paragraph 5.5.4 Rate 1/2 4.4dB	10^{-5}	8×10^{-6}	1.2×10^{-5}	9.606×10^{-6} pass
Paragraph 5.5.5 Rate 1/3 4.1 dB	10^{-5}	8×10^{-6}	1.2×10^{-5}	1.124×10^{-6} pass

TEST 6: Initial Synchronization

TEST	TRIAL	PASS/FAIL
Paragraph 5.6.2 Initial synchronization maximum = 120,000	1. 36,000 symbol times	~~36,000~~ PASS
	2. 12,000	PASS
	3. 36,000	PASS
	4. 66,000	PASS
	5. 30,000	PASS
	6. 48,000	PASS
	7. 72,000	PASS
	8. 18,000	PASS
	9. 54,000	PASS
	10. 36,000	PASS

* STATE COUNT IS 119 FOR 29 OUT OF 30 STATE COUNTS WHEN 30 BIT WIDTH INPUT PULSE IS NOT SYNCHRONOUS WITH DE INTERLEAVER SYNC STATE 0. THE REMAINING STATE COUNT IS 149, WITH THE STATE COUNT POSITION BEING RANDOM. WHEN THE 30 BIT WIDTH INPUT PULSE IS SYNCHRONOUS WITH THE DEINTERLEAVER SYNC STATE 0, ALL 30 STATE COUNTS ARE 119.

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

Test Engineer Steven M. Gaud NASA Representative Glenn W. Heyer
DENVER W HERR

Date 3-5-87

TEST 7: Resynchronization

TEST	TRIAL	PASS/FAIL
Paragraph 5.7.2.a Resync after BITSLIP w/o interleaver. maximum = 500	1. 200 symbol times 2. 100 3. 200 4. 100 5. 100	Pass Pass
Paragraph 5.7.2.c Resync after inversion w/o interleaver maximum = 500 $E_b/N_0 = 4.4dB$	1. 0 2. 0 3. 0 4. 0 5. 0	Pass Pass
Paragraph 5.7.2.e Resync after BITSLIP with interleaver maximum = 8,000	5.7.2.e 1. 1000 symbol times 2. 2000 3. 2000 5.7.2.f 1. 3000 2. 3000 3. 3000	Pass Pass Pass Pass Pass Pass

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

Test Engineer Steven J. Gaud NASA Representative Dennis W. Herr
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Date 3-5-81

TEST 8: Automated Test Program

TEST	PASS/FAIL
Test 1	PASS
Test 2	PASS
Test 3	PASS

Acceptance Test Procedure Data Sheet
for
Decoding Simulation System

Test Engineer Steven M. Gardner NASA Representative Dennis W. Herr
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Date 3-5-81

TEST 9: Government Data Test (Paragraph 6)

See attachments (2 sheets)

TEST	RESULTING BER EXPECTED	MIN	MAX	PASS/FAIL
CASE 1. SOFT DECISION w/INT. - LOSS OF DECODER SYNC				N/A
2. SOFT DECISION w/o/INT. - LOSS OF DECODER SYNC				
3. HARD DECISION w/INT. - 1.9×10^{-4}				
4. HARD DECISION w/o/INT - 1.9×10^{-4}				
CASE 2. SOFT DECISION w/INT. - LOSS OF DECODER SYNC				
9. SOFT DECISION w/o/INT. - LOSS OF DECODER SYNC				
10. HARD DECISION w/INT. - 1×10^{-4}				
HARD DECISION w/o/INT. - 4.1×10^{-3}				
CASE 3. SOFT DECISION (DECODER IN SYNC) w/INT. - 2.6×10^{-5}				
w/o INT. - 2.8×10^{-5}				
CASE 4. SOFT DECISION w/INT - DECODER OCCASIONALLY DROPPED SYNC				
2.9×10^{-5} BETWEEN LOSS OF SYNC				
w/o/INT. - LOSS OF DECODER SYNC				
CASE 5. SOFT DECISION w/INT. - 1.3×10^{-5}				
w/o INT. - 1.4×10^{-5}				

Case 1

#2
0,1,5,16,44,109,229,3692
1671,128,125,124,124,125,128,1671
243,13
243,13
0,0
Infinite CW RFI In-band; Rate 1/2
PULSE/SYMBOL = 1
PREDICTED PE = 1E-4
^G

Hard Decision
with INT $\approx 1.9 \times 10^{-4}$
w/o INT $\approx 1.9 \times 10^{-4}$

Soft Decision
w/o INT ~~[illegible]~~ LOSS OF DECODER SYNC
w INT LOSS OF DECODER SYNC

Case 2

#2
0,1,5,16,44,109,229,3692
1671,128,125,124,124,125,128,1671
253,3
253,3
0,3
Infinite CW RFI In-band; Rate 1/2
PULSE/SYMBOL = 4
PREDICTED PE (WITH INTERLEAVER) = 1E-4
^G

~~[illegible]~~ WITHOUT INT
SOFT DECISION
DECODER LOSING SYNC
WITH/WITHOUT INT.
HARD DECISION WILL
MAINTAIN SYNC WITHOUT INT
4.1×10^{-3}
3.1×10^{-9} WITH INTERLEAVER

Case 3

#2
0,2,9,37,111,263,488,3186
484,221,276,327,366,388,388,1647
238,13
238,18
0,0
NOISE RFI; 45 DBW E IRP; Rate 1/2
PULSE/SYMBOL = 1
PREDICTED PE = 2.6E-5
^G

SOFT DECISION
DECODER IN SYNC
INT OUT 2.8×10^{-5}
INT IN 2.6×10^{-5}

Case 4

SOFT DECISION

INT IN DECODER Dropping Sync
INSYNC ≈2.9×10⁻⁵
INT OUT DECODER DROPPING SYNC

#2
0,2,9,37,111,263,488,3186
484,221,276,327,366,388,388,1647
252,4
252,4
0,4
NOISE RFI; 45 DBW EIRP; Rate 1/2
PREDICTED PE (WITH INTERLEAVING = 2.6E-5)
^G

Case 5

Soft Decision — Decode in Sync
INT OUT 1.4×10⁻⁵
INT IN 1.3×10⁻⁵

#7
5,18,61,167,356,593,775,2121
5,18,62,168,356,593,774,2121
6,20,65,173,359,590,764,2120
17,39,99,213,378,558,683,2110
1829,74,73,73,73,73,74,1829
299,120,228,287,340,380,400,1992
1147,283,304,315,315,304,283,1147
188,18,28,11,3,4,3
188,18,28,11,3,4,3
188,18,28,11,3,4,3
188,18,28,11,3,4,3
188,18,28,11,3,4,3
188,18,28,11,3,4,3
188,18,28,11,3,4,3
0,0,0,0,0,0,0
0,0,0,0,0,0,0
0,0,0,0,0,0,0
0,0,0,0,0,0,0
0,0,0,0,0,0,0
0,0,0,0,0,0,0
0,0,0,0,0,0,0
ST case; Rate 1/3
PULSE/SYMBOL = 1
PREDICTED PE = 1E-5
^G

OPERATING INSTRUCTIONS

FOR

TRANSITIONAL PROBABILITY GENERATOR

(T P G MANUAL)

APPENDIX B

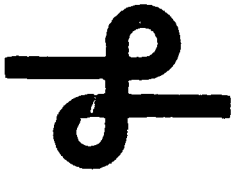
TM 21371
March 1981

OPERATION AND MAINTENANCE MANUAL

FOR

TRANSITION PROBABILITY GENERATOR

LINKABIT Part No. 21371



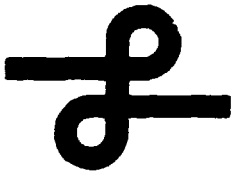
LINKABIT Corporation

OPERATION AND MAINTENANCE MANUAL

FOR

TRANSITION PROBABILITY GENERATOR

LINKABIT Part No. 21371



LINKABIT Corporation
A M/A-COM Company
3033 Science Park Road
San Diego, CA 92121
714/453-7007
TWX 910-337-1277

WARRANTY

LINKABIT Corporation warrants the Transition Probability Generator to be free from defects in material, workmanship, and construction arising from normal usage. Its obligation under this Warranty is limited to replacing, or at its option, repairing any such defective equipment, which after regular installation and under normal usage and service, shall be returned within one (1) year from the date of original purchase to LINKABIT Corporation and which shall be found to have been thus defective in accordance with the policies established by LINKABIT Corporation.

LINKABIT Corporation assumes no liability for failure to perform or delay in performing its obligations with respect to this Warranty if such failure or delay results, directly or indirectly, from any cause beyond its control, including but not limited to, acts of God, acts of government, floods, fires, shortage of materials and labor and/or transportation difficulties.

This Warranty is expressly in lieu of all other agreements and warranties, express or implied, and LINKABIT Corporation does not authorize any person to assume for it the obligations contained in this Warranty and neither assumes nor authorizes any representative or other person to assume for it any other liability in connection with such equipment.

The Warranty shall not apply to any equipment which shall have been repaired or replaced by anyone else other than LINKABIT Corporation or which has been subject to alteration, misuse, negligence or accident, or to any equipment which shall have had the serial number or name altered, defaced or removed.

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SECTION 1

INTRODUCTION

1.1 SCOPE

This manual describes the Transition Probability Generator, hereinafter referred to as the TPG (figure 1-1). It includes installation, operation, and maintenance information. A description of the equipment is contained in section 1. Section 2 provides the installation instructions. Operating instructions are provided in section 3. Theory of operation is in section 4. Maintenance instructions are included in section 5.

1.2 PURPOSE AND FUNCTION

The TPG is a calculator-controlled noise generator that can be used to simulate the effects of noise channels on encoded or interleaved data. The TPG produces 3-bit soft decision outputs whose distributions can be programmed on an Hewlett-Packard 9825 calculator to simulate a variety of noise environments. These 3-bit outputs are added to the encoded data stream and are then returned to the decoder.

The probabilities of each 3-bit output are specified to 12-bit accuracy. The TPG can provide up to 32 output distributions or states, with probabilities of transitions between any pair of states determined with 8-bit accuracy. There is also provision to hold any of the states for up to 256 clock cycles. It is also possible to hold one output in a particular state.

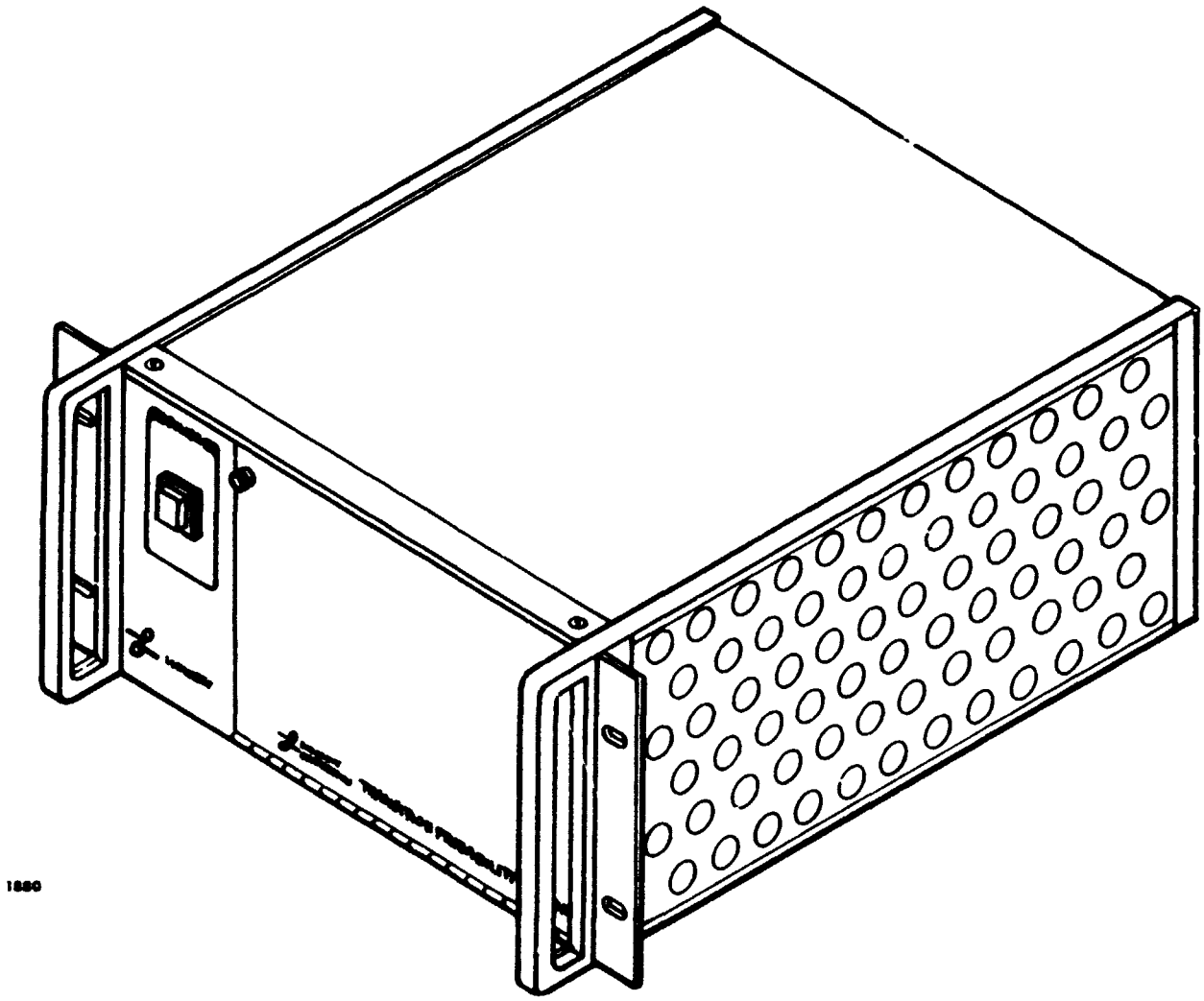


Figure 1-1. Transition Probability Generator

The TPG is controlled by an HP9825 calculator which can also control the Bit Error Rate (BER) Test Set, LINKABIT PN 21270. Probability distribution data is created on an outside computer and downloaded to the HP9825. Alternately, probability distribution data can be entered manually from the calculator keyboard. The calculator creates images of the TPG's lookup tables and loads the TPG. The calculator can then be programmed to control the BER test set and run tests automatically. The TPG Program Cassette contains all the programs necessary to run the TPG.

1.3 DESCRIPTION

The TPG is a standard 19-inch, rack-mountable enclosure weighing 30 pounds. There is a plug-in circuit card assembly (CCA) inside the hinged front cover. There are three switches along the front edge of the CCA that are accessible when the front panel is hinged down. The chassis also contains a power supply and a fan. All input/output and clock connections are made by means of rear panel Cannon connectors (DL2-96RW). Refer to figure 1-2 and table 1-1. See figure 1-3 for data timing.

1.4 TEST EQUIPMENT

A Hewlett-Packard 1610A logic analyzer or equivalent is required to check that the TPG is operating properly.

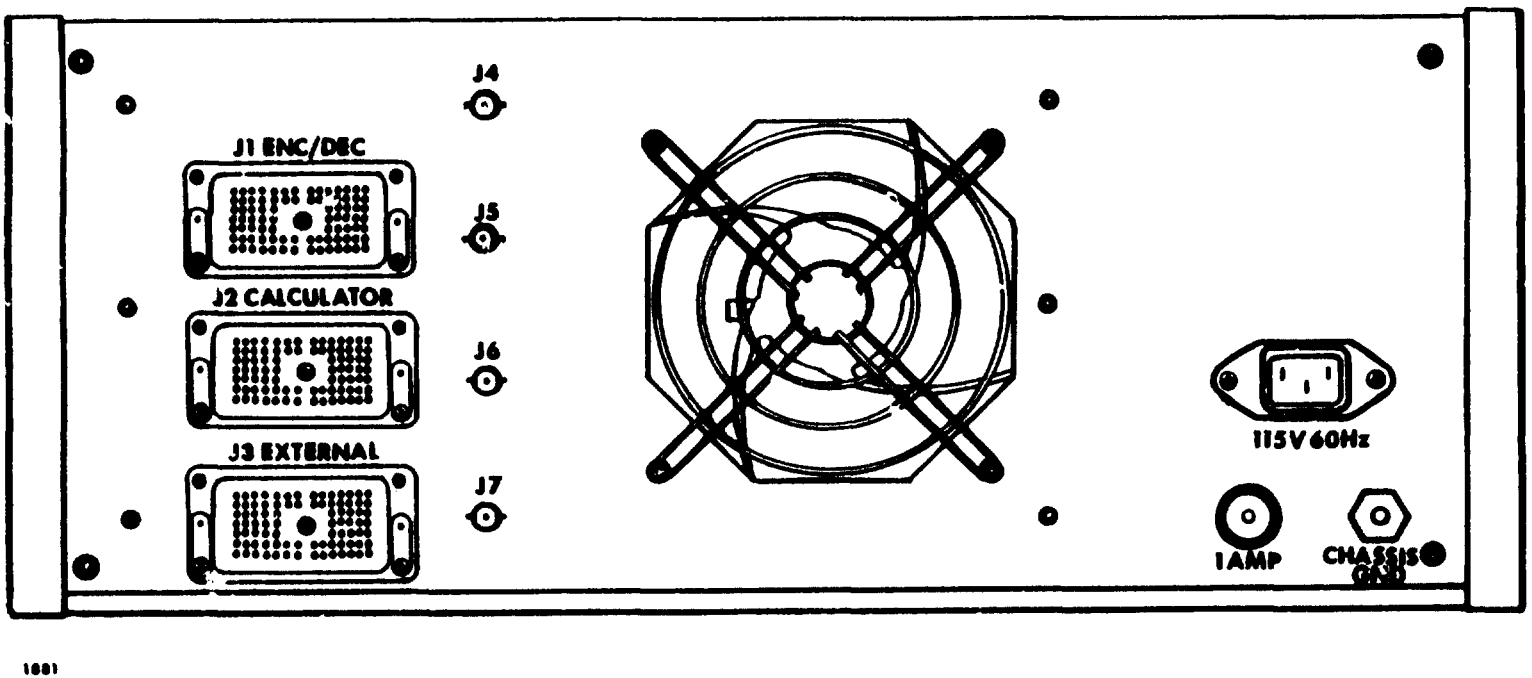
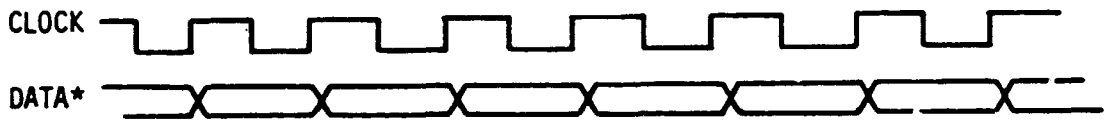


Figure 1-2. TPG Rear View

Table 1-1. Input/Output Interface

Signal	Interface Logic Specification
Input Signals and Clocks	RS-422 AMD-26LS32 line receivers terminated in 100Ω
Output Signals and Clocks	RS-422 AMD-26LS31 line drivers
Calculator Inputs/Outputs	TTL with 1 KΩ pull-up resistors



*INPUT PORT HAS ONE DATA CHANNEL.
OUTPUT PORT HAS THREE CHANNELS: ONE FOR DATA AND TWO QUALITY BITS.

1912

Figure 1-3. Data Timing

1.5 ASSOCIATED EQUIPMENT

The associated test equipment shown in table 1-2 is required to complete the system in which the TPG operates.

Table 1-2. Associated Equipment

Model	Nomenclature	Manufacturer
21270	Bit Error Rate Test Set	LINKABIT
HP9825	Calculator	Hewlett-Packard
LV7017B	Encoder-Decoder	LINKABIT
HP98032A	Parallel I/O Bus	Hewlett-Packard
HP98034	Instrument Bus	Hewlett-Packard
HP98036	Serial I/O Interface Bus	Hewlett-Packard

SECTION 2

PREPARATION FOR USE AND INSTALLATION INSTRUCTIONS

2.1 UNPACKING

The TPG is packaged in a plastic bag and an inner cardboard carton which is placed in an outer carton. The outer carton contains preformed plastic foam with a recess for the inner carton, the Operation and Maintenance Manual, and the program cartridge. A sheet of plastic foam is placed on top of the inner carton to complete the cushioning on all sites of the inner carton. To remove the TPG from the cartons, proceed as follows:

CAUTION

When cutting the tape on the inner carton, do not allow the cutting tool to penetrate the carton and damage the TPG.

1. Cut or tear the sealing tape from the top of the outer carton.

2. Remove the sheet of plastic foam which covers the inner carton. Observing the previous caution, cut or tear the sealing tape from the inner carton.

3. Remove the TPG from the inner carton. Do not remove plastic cover until ready for inspection. If the TPG is not to be inspected immediately, store in a safe, clean, dry place pending inspection.

2.2 INSPECTION UPON RECEIPT

Inspect unpacked equipment upon receipt as follows:

1. Inspect the equipment for damage incurred during shipment.

2. Check the equipment against the packing list shipped with the equipment to ensure that the shipment is complete.

2.3 INSTALLATION INSTRUCTIONS

2.3.1 RACK REQUIREMENTS

The TPG is designed for standard 19-inch rack mounting. It is packaged in a 7-inch high by 19-inch wide by 17-inch deep enclosure. The unit may be operated in any orientation providing that the intake holes on the side panels and the fan have unimpeded access to intake air.

2.3.2 ELECTRICAL CONNECTIONS

Required power is 115 volts at 60 Hz. A 1 amp fuse is located on the rear panel. It is recommended that the unit not be operated without adequate grounding.

2.3.3 CONNECTOR PINS

Signal names for connectors J1, J2, and J3 are provided in tables 2-1, 2-2, and 2-3.

Table 2-1. J1 Connector

ENCODER-DECODER J1 Pin Number	Signal (RS-422 Differential TTL)
C1	CLOCKIN +
E1	DATAIN +
G1	SIGNOUT +
H1	MSBOUT +
K1	LSBOUT +
M1	CLOCKOUT +
C2	CLOCKIN -
E2	DATAIN -
G2	SIGNOUT -
H2	MSBOUT -
K2	LSBOUT -
M2	CLOCKOUT -

Table 2-2. J2 Connector

CALCULATOR J2 Pin Number	Signal (Single ended TTL)
C1	PFLG
D1	PCTL
E1	CTL1
F1	CTL0
C2	GND
D2	GND
E2	GND
J2	DO2
K2	DO3
L2	DO4
M2	DO5
N2	DO6
P2	DO7
K5	DO8
L5	DO9
M5	D10
N5	D11
P5	D12
D6	PRESET
N6	DO0
P6	DO1

Table 2-3. J3 Connector

EXTERNAL J3 Pin Number	Signal (RS-422 Differential TTL)
C7	CLOCKOUT +
C8	CLOCKOUT -
M7	DATAOUT +
M8	DATAOUT -
K1	CLOCKIN +
K2	CLOCKIN -
E1	SIGNIN +
E2	SIGNIN -
G1	MSBIN +
G2	MSBIN -
H1	LSBIN +
H2	LSBIN -

2.3.4 DATA TERMINAL CONFIGURATION

To enable data terminal configuration proceed as follows:

1. Insert the three calculator interface cards into the input/ouput slots at the rear of the HP9825 calculator. They may be in any order.

2. Connect the Bit Error Rate Test Set LV7017B, HP9825, and TPG as shown in figure 2-1.

2.3.5 EXTERNAL CHANNEL CONFIGURATION

The TPG may be bypassed to an external channel connecting a modem to the EXTERNAL jack on the TPG. The signals on this interface have RS-422 levels. The pin signals at this interface are defined in table 2-1. The connector is a Cannon DL2-96P. To enable an external channel, proceed as follows:

1. Lower the front panel, to gain access to the BYPASS switch.

2. Set the BYPASS switch on the TPG circuit card to BYPASS.

2.3.6 TEST SWITCHES S2 AND S3

Switches S2 and S3 provide two error sources useful for testing the decoder/deinterleaver. Set the switches as follows:

1. Set switch S2 to ON to delay data by one clock.

2. Set switch S3 to ON to invert the data.

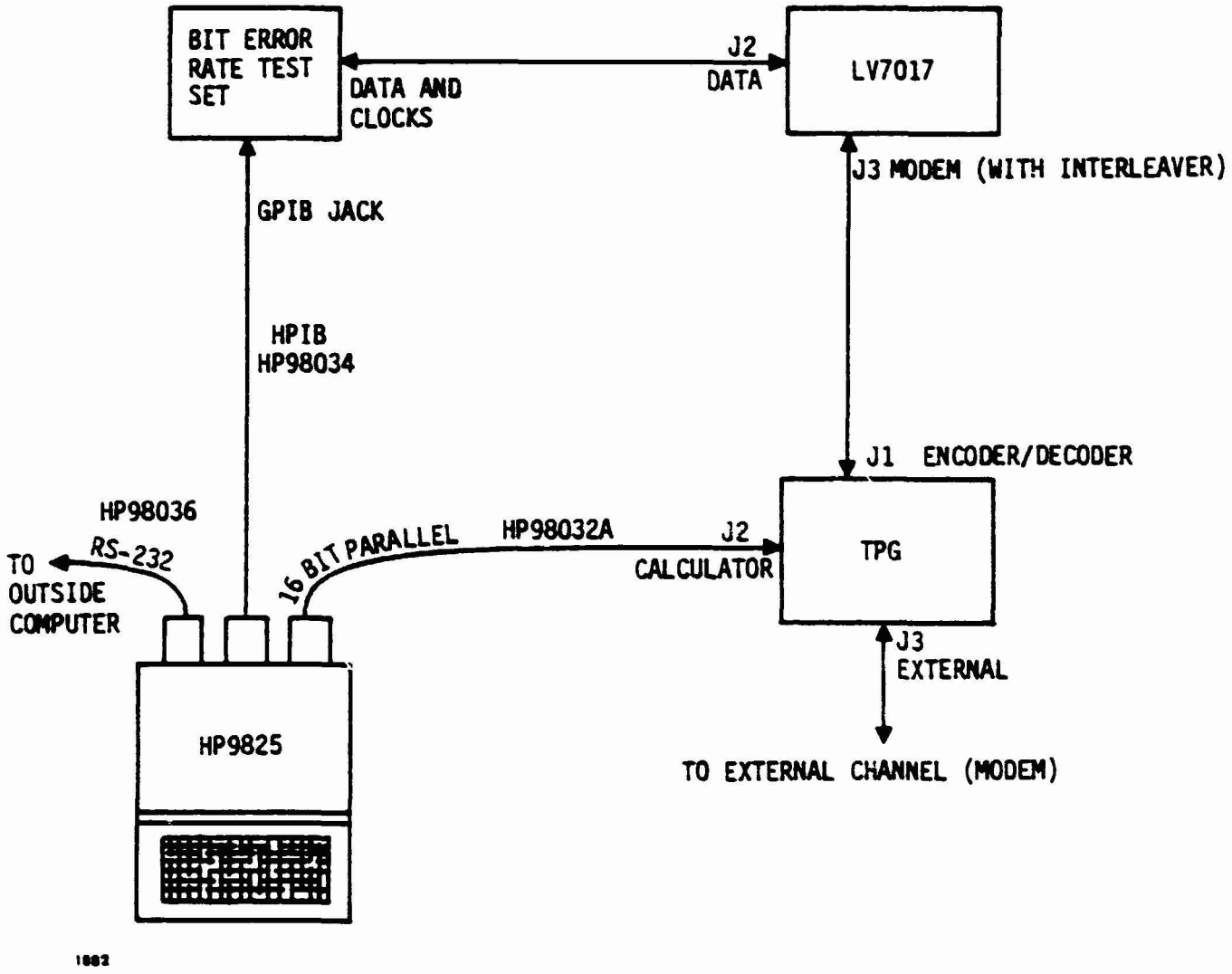


Figure 2-1. System Block Diagram

SECTION 3

OPERATING INSTRUCTIONS

3.1 GENERAL

The TPG is controlled by the calculator. It is necessary that the operator have previous experience using the calculator. The operator should be able to perform the following:

1. Load the special function keys by loading and running the loader program.
2. Enter data into the calculator when prompted to do so.
3. Correct typing mistakes using editing keys.
4. Recover after a calculator error has occurred.

Program cassette TC is necessary to operate the TPG. It contains the DOWNLOAD, ARRAYS, LOADTEST, MANUAL, CATALOG, and RUNTEST programs, the definitions of the special function keys, and two test distributions.

3.2 SPECIAL FUNCTION KEYS

The definitions of the special keys are contained in file 1 on track 0. Keys f2 through f5 do not affect the operation of the calculator or any program being executed. Following is a list of the special function keys:

f0: YES For yes/no answers

f1: NO For yes/no answers

f2: START Starts the TPG

f3:	START	Starts the TPG
f4:	STOP	Stops the TPG; can be started again with either START.
f5:	RESET	Returns the TPG to power up condition; must be reloaded.
f6:	DOWNLOAD	Loads the DOWNLOAD program from the program cassette.
f7:	ARRAYS	Loads the ARRAYS program from the program cassette.
f8:	LOADTEST	Loads the LOADTEST program from the program cassette.
f9:	MANUAL	Loads the MANUAL program from the program cassette.
f10:	CATALOG	Loads the CATALOG program from the program cassette.
f11:	RUNTEST	Loads the RUNTEST program from the program cassette.

3.3 DATA CASSETTE FILE FORMAT

A data file for each test consists of six consecutive files on a data cassette. In each group of six, the first contains the raw data received from the outside world via the DOWNLOAD program, or entered manually via the MANUAL program. The next five files are created by the ARRAYS program from the data in the first file. These last are used by the LOADTEST program to load the Test Set.

When a program asks for a file number, the number it expects is that of the FIRST file in each set of six (i.e., the 3400-byte file). The other files will be accessed relative to this one.

3.4 DATA CASSETTE CATALOG

The CATALOG program prints the headings of all the files on a data cassette. To use CATALOG program, proceed as follows:

1. Insert program cassette.
2. Depress s/f key f10 (CATALOG).
3. Depress RUN.
4. When INSERT DATA CASSETTE is displayed:
   - Insert a data cassette.
   - Depress CONTINUE.
5. The program will then search through the tape and print the headings of all the data files.

3.5 PROGRAM CASSETTE

The program cassette contains the DOWNLOAD, ARRAYS, LOADTEST, MANUAL, CATALOG, and RUNTEST programs, the definitions of the special function keys, and two test distributions.

3.5.1 RUNNING PROGRAMS

To use the programs on the program cassette, proceed as follows:

1. Insert the program cassette.
2. Turn the calculator and the TPG on. The calculator will automatically execute a "ldp 0" to load and run the first program on the cassette, which prints a message and loads the special function keys.
3. Depress the RESET s/f key (f5) to initialize the random number generators.
4. Use the s/f keys to select program.

5. To go to another program, re-insert the program cassette, if it has been removed.

3.5.2 TESTING

The normal sequence of steps to run a test is provided in table 3-1. Each step in table 3-1 is described in paragraphs 3.5.2.1 through 3.5.2.7.

3.5.2.1 **MARKING DATA CASSETTES** - To mark data cassettes, proceed as follows:

1. To mark a new cassette, insert the cassette and rewind it (REWIND key). This will position the tape at the beginning of track 0. At least four, possibly five, sets of files will fit on each track.

2. To mark a set of six files, use the following sequence of statements, and repeat for each set of six:

    a. mrk 1,3400 (EXECUTE)

    b. mrk 1,730 (EXECUTE)

    c. mrk 3,8220 (EXECUTE)

    d. mrk 1,80 (EXECUTE).

3. When track 0 is marked, rewind the tape and type: trk 1 (EXECUTE). This positions the tape at the beginning of track 1 and is now ready to be marked as described above. All six files of each set must be on the same track.

4. When marking a used cassette, make certain that the tape is positioned after the last file to be saved before doing any marking, since marking erases old files. To determine the position of the last file, perform the following procedures:

    a. Rewind the tape.

Table 3-1. Test Steps

Step	Action	Paragraph
1	Mark data cassettes	3.5.2.1
2	Create input file on outside computer	3.5.2.2
3	Download the file to the calculator (DOWNLOAD), or enter data manually (MANUAL)	3.5.2.3 3.5.2.4
4	Create RAM images for TPG (ARRAYS)	3.5.2.5
5	Load the TPG (LOADTEST)	3.5.2.6
6	Run the test or load and run an automated series of tests (RUNTEST)	3.5.2.7

b. Select a track.

c. Type: tlist (EXECUTE). The last file number will be identified by a row of zeroes.

d. Type: fdf X (where X is the number of the last file) and EXECUTE. This will position the tape at the last file, ready for marking.

3.5.2.2 INPUT FILE FORMAT - The input file contains all the information concerning the output and state transition probabilities for use by the TPG. It also includes an identifying heading to be printed with the test results.

NOTE

The input file must be unnumbered and free of extraneous control characters.

The input file has the following seven parts:

1. Beginning-of-file mark
2. An integer representing the number of states
3. The output probabilities for each state
4. The state transition probabilities
5. Integers indicating the time to hold each state
6. Heading text
7. End-of-file mark.

3.5.2.2.1 Delimiters - In general, it does not matter whether data items appear on separate lines or grouped together on lines, because the HP9825 considers any nonspace, nonnumerical character a delimiter. Data items that appear on the same line should be

separated by delimiters (i.e, commas) and terminated with a LF. Do not use both a comma and a LF at the end of a line; the calculator will interpret this as another data item (zero).

3.5.2.2.2 Line Terminators - The HP9825 does not understand CR (ASCII 13); when it encounters one, it is ignored. Therefore, lines can be terminated with either LF (ASCII 10) or CR/LF.

3.5.2.2.3 Format -

3.5.2.2.3.1 First Line - The first line consists of a beginning-of-file mark: a number sign # (ASCII 35) followed by an integer N from 1 to 32 inclusive indicating the number of states. There are no delimiters in between. The DOWNLOAD program starts to read data immediately after encountering the #, therfore, anything that appears before it is ignored. N is used to determine how much probability data follows.

3.5.2.2.3.2 Output Probabilities - These are a total of 8*N integers in the range 0 to 4096 representing the probability of each possible output in each state, where 4096 indicates a probability of 1.0 and 0 is a probability of 0.0. They must be arranged in the following order:

State Number	Output
1	011, 010, 001, 000, 100, 101, 110, 111
2	011, 010, 001, 000, 100, 101, 110, 111
:	
:	
N	011, 010, 001, 000, 100, 101, 110, 111

This data may be delimited in any convenient manner. The sum of each state must be 4096.

3.5.2.2.3.3 State Probabilities - These are a total of N*N integers in the range 0 to 256 representing the probability of the transition from a given state to any other state. In this case, 256 indicates a probability of 1.0. They must be arranged in the following order:

From State	To State
1	1, 2, 3, ... N
2	1, 2, 3, ... N
:	
:	
N	1, 2, 3, ... N

This may also be delimited in any convenient manner. The sum of each state must be 256.

3.5.2.2.3.4 Hold Length - These are a total of N integers from 0 to 255, representing the number of clocks a given state is to be held. A 0 indicates that this particular state will not be held. All N states must be included, in order. If, when reaching a particular state, the output is to be held also, add 256 to its number.

3.5.2.2.3.5 Heading Text - This part consists of up to 720 characters (including control characters) to be used as a heading to identify the test. This text will be printed on the HP9825's internal printer exactly as it appears here, thus each line is limited to 16 characters (the width of the printer). Any

additional characters over 16 will not be printed. About 40 lines of text can be included.

3.5.2.2.3.6 End-of-File Mark - The end-of-file mark is a BELL (control G, ASCII 7). It need not appear on its own line. The calculator terminates its input operation when it sees this character.

3.5.2.3 DOWNLOADING DATA

The DOWNLOAD program gets the input file from the outside world, reformats it, and stores it on a data cassette.

To use DOWNLOAD, proceed as follows:

1. Prepare the input files.

2. Set up the calculator. Depress s/f key f6 (DOWNLOAD) to load the program.

3. Prepare the outside computer and connect it to the calculator via the RS-232 interface, so that all that is necessary to start the download is to enter a single command (such as "TYPE FILE.NAME"). The RS-232 interface requires the following:

   a. 1 stop bit

   b. 7 bit ASCII characters, plus

   c. 1 (odd) parity bit

   d. 2400 baud

   Use halfduplex mode and make sure that the file is free of extraneous control characters (page marks, form feeds, etc.).

4. Depress RUN.

5. When INSERT DATA CASSETTE is displayed, proceed as follows:

    a. Insert the cassette on which this file is to be stored.

    b. Depress CONTINUE.

6. When WHICH TRACK (0/1)? is displayed, proceed as follows:

    a. Enter the track number for this file.

    b. Depress CONTINUE.

7. When WHICH FILE? is displayed, proceed as follows:

    a. Enter the file number for this file.

    b. Depress CONTINUE.

    The program will check to see if it is a valid file. If it is the wrong type, size, or not marked at all, a message to that effect will be displayed. Depress CONTINUE to return to the point where it asks for a track number. If the program finds data in the file already, depress YES (f0) to write over it, or NO (f1) to enter a new file number.

8. When COMMAND? is displayed, proceed as follows:

    a. Enter the command that will start the download.

    b. Depress CONTINUE.

    Type the command exactly as it would appear on a computer terminal. The calculator will supply a CR/LF at the end.

9. The calculator will print the first 100 characters of the heading as a check that the download succeeded. If the messages "sum not 4096 in state X" or "sum not 256 in state X" appear, there was an error in the input file, which must be corrected and reloaded.

10. To do another download, prepare the next input file and go to step 3.

11. Proceed to ARRAYS, paragrah 3.5.2.5.

3.5.2.4 MANUAL ENTRY OF DATA - The MANUAL program can be used to manually enter the distribution data, if desired. If may be easier than DOWNLOAD if there are only a few states to enter. The data is entered in exactly the same format as in the input file (paragraph 3.5.2.2).

To use MANUAL, proceed as follows:

1. Insert program cassette.

2. Depress s/f key f9 (MANUAL).

3. Depress RUN.

4. When NUMBER OF STATES? is displayed, proceed as follows:

    a. Enter integer number of states from 1 to 32.

    b. Depress CONTINUE.

5. When PROBABILITY? is displayed, proceed as follows:

    a. Enter an integer from 0 to 4096 representing the output probability.

    b. Depress CONTINUE.

    The output probabilities must be entered in the same order as in the input files (paragraph 3.5.2.2). The program will continue to ask for output probabilities until all N states are complete. If the message "sum not 4096" appears, the program will ask for that state again.

6. When TRANSITION PROBABILITY? is displayed, proceed as follows:

a. Enter an integer from 0 to 256 representing the transition probability between the two states.

b. Depress CONTINUE.

The state transition probabilities must be entered in the same order as in the input file (paragraph 3.5.2.2). The program will continue to ask for transition probabilities until all N states are complete. If the message "sum not 256" appears, the program will ask for that state again.

7. When NUMBER OF CLOCKS? is displayed, proceed as follows:

   a. Enter an integer from 0 to 255 representing the number of clock cycles this state is to be held. (Enter 256-511 if the output is to be held also.)

   b. Depress CONTINUE.

   The program will continue to ask for input until all N states are complete.

8. When LINE? is displayed, proceed as follows:

   a. Enter up to 16 characters of heading text.

   b. Depress CONTINUE.

9. When ANOTHER LINE? is displayed, depress YES (f0) to enter another line, or NO (f1) if finished. Up to 720 characters of heading can be entered.

10. When INSERT DATA CASSETTE is displayed proceed as follows:

    a. Insert a (premarked) data cassette.

    b. Depress CONTINUE.

11. When TRACK? is displayed, proceed as follows:

    a. Enter the track number of the desired file.

b. Depress CONTINUE.

12. When FILE NUMBER? is displayed, proceed as follows:

    a. Enter the file number (premarked 3400 bytes).

    b. Depress CONTINUE.

    If the file is the wrong size, type, or not marked at all, a message will be displayed. Depress CONTINUE to enter a new file. If there is data in the file already, depress YES (F0) to write over it, or NO (f1) to enter a new one.

13. The program will display DONE when finished. Proceed to ARRAYS (paragraph 3.5.2.5).

3.5.2.5 GENERATING RAM IMAGES - The ARRAYS program takes the input file created by DOWNLOAD and generates the arrays that will be loaded into the TPG RAMs by the LOADTEST program.

To use ARRAYS, proceed as follows:

1. Insert the program cassette.
2. Depress s/f key f7 (ARRAYS).
3. Depress RUN.
4. When INSERT DATA CASSETTE is displayed, proceed as follows:

    a. Insert the data cassette on which the data is to be stored.

    b. Depress CONTINUE.

5. When WHICH TRACK (0/1)? is displayed, proceed as follows:

    a. Enter the track number of the input file.

b. Depress CONTINUE.

6. When WHICH FILE? is displayed, proceed as follows:

   a. Enter the file number of the input file.

   b. Depress CONTINUE.

   The program checks for the existence and correct type of file, and displays a message if incorrect. Depress CONTINUE to return to the point where it asks for the track number and enter a new file.

7. This program creates images of the RAM contents and stores them in the files following the input files. The files must be premarked. When DONE is displayed, the program is finished.

8. To do another set of arrays, go to step 3.

9. Proceed to LOADTEST.

3.5.2.6 LOADING TPG RAMs - The LOADTEST program loads the TPG RAMs. To use LOADTEST, proceed as follows:

1. Insert the program cassette.

2. Depress s/f key f8 (LOADTEST).

3. Depress RUN.

4. When INSERT DATA CASSETTE is displayed, proceed as follows:

   a. Insert the data cassette on which the data files are located.

   b. Depress CONTINUE.

5. When TRACK? (0/1) is displayed, proceed as follows:

   a. Enter the track number of the input files.

   b. Depress CONTINUE.

6. When NUMBER OF FIRST FILE? is displayed, proceed as follows:

    a. Enter the number of the first of the set of six files.

    b. Depress CONTINUE.

    The program checks for the existence and correct type of file. If incorrect, depress CONTINUE to start over and enter a new file.

7. The program first prints the header, then loads the TPG RAMs. When DONE is displayed, the program is finished.

8. Depress START (s/f key f2) to start the TPG.

9. During a test, the BITSLIP and INVERT switches on the TPG circuit card (accessible through the front panel) may be used to manually introduce a one-bit delay or phase inversion.

3.5.2.7 AUTOMATED TESTS - The RUNTEST program stores parameters for a series of tests to be run under the control of the HP9835 calculator. The program first asks for the parameters, then TPG initializes the Bit Error Rate Tester (FLERT), and runs the tests.

To use RUNTEST, proceed as follows:

1. Insert program cassette.

2. Depress s/f key f11 (RUNTEST).

3. Depress RUN.

4. When INSERT DATA CASSETTE is displayed, proceed as follows:

    a. Insert a data cassette that contains ALL the tests you wish to run.

b. Depress CONTINUE.

5. When ENTER NUMBER OF TESTS is displayed, proceed as follows:

   a. Enter the number of tests.

   b. Depress CONTINUE.

6. When FILE NUMBER and TRACK NUMBER are displayed, enter the file and track numbers of the data file, depressing CONTINUE after each. This program WILL NOT check for existence and correctness of the files.

7. When SYMBOL CLOCK is displayed, proceed as follows:

   a. Enter the symbol rate in symbols/second.

   b. Depress CONTINUE.

8. When PATTERN is displayed, proceed as follows:

   a. Enter 0, 4, 8, 11, 15, or 16 for the data pattern.

   b. Depress CONTINUE.

9. When INVERT is displayed, proceed as follows:

   a. Depress YES (f0) for an inverted data pattern, or

   b. Depress NO (f1) for a normal pattern.

10. When LENGTH OF TEST (bits) is displayed, proceed as follows:

    a. Enter the duration of the test in information bit times.

    b. Depress CONTINUE.

11. Repeat steps 6 through 10 for each test. These parameters for each test will be printed on the calculator's printer. If there is an error, start over from step 3.

12. When all tests are entered, the program will pause.

13. Depress CONTINUE when ready to begin testing.

14. The program will load the TPG.

15. The program will initialize the FLERT.

16. The program will run the test for the specified time.

17. At the conclusion, the bit count, error count and BER will be printed.

18. The program will repeat steps 13 through 16 for each test, and will display TESTS COMPLETED when finished.

SECTION 4

THEORY OF OPERATION

4.1 OVERALL THEORY OF OPERATION

The TPG consists of four RAM lookup tables, two random number generators and associated loading logic. A block diagram of the TPG is shown in figure 4-1. The HP9825 calculator determines the contents of the lookup tables from probability distribution data provided to it.

4.1.1 STATE TABLE

The State lookup table determines which of the 32 possible distributions to use next, given the previous state and an 8-bit random number.

4.1.2 HOLD STATE TABLE

The Hold State lookup table determines how long to hold a particular state given that state. The Hold State holds a state by disabling the state register, while a counter counts out the number of clocks provided by the Hold State lookup table.

4.1.3 REGION TABLE

The Region lookup table contains the joint cumulative distribution of all possible states. When superimposed, the cumulative distributions of the outputs in each state will form up to 225 intervals. A 12-bit random number selects one of these intervals.

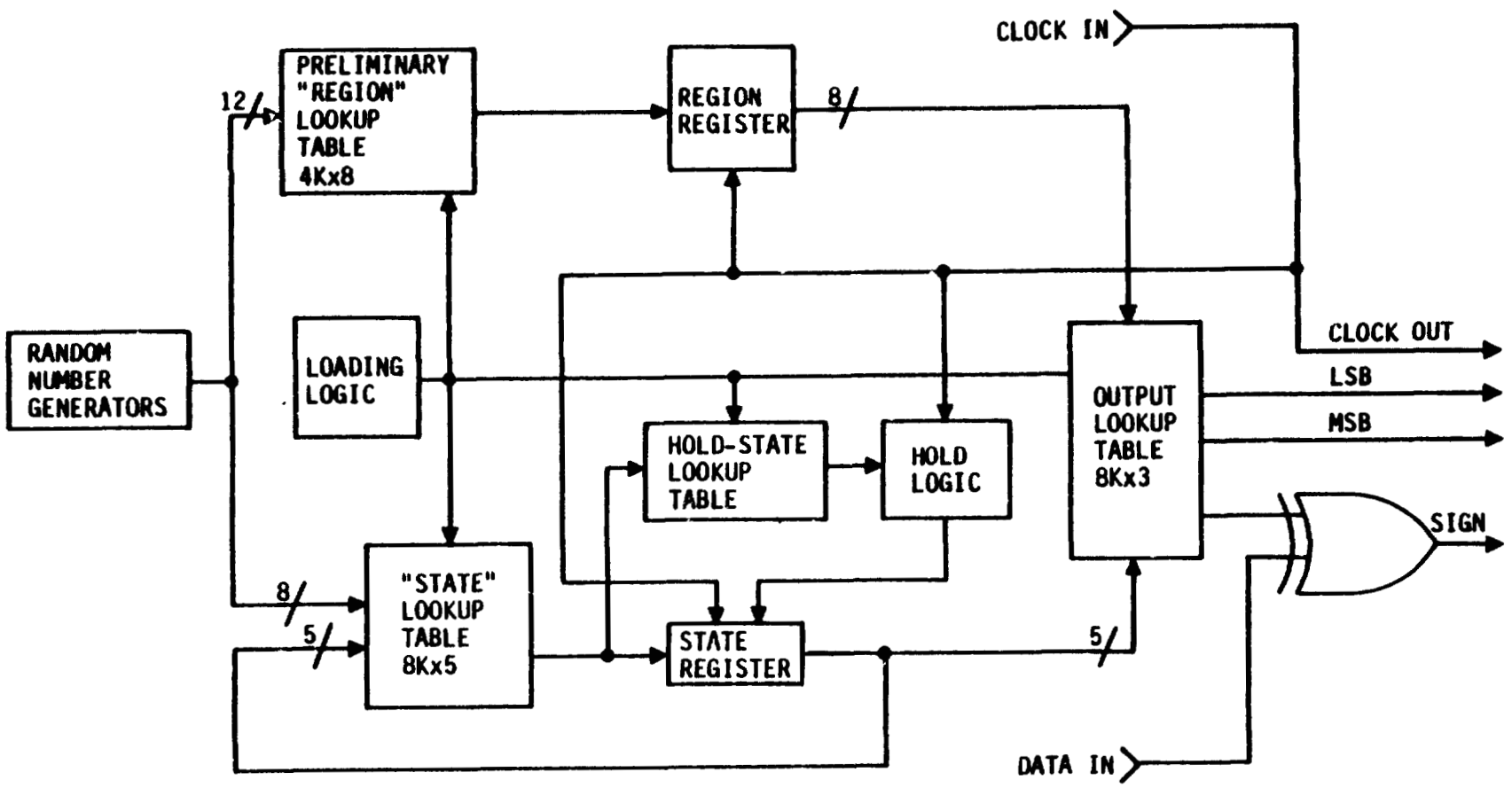


Figure 4-1. TPG Block Diagram

4.1.4 OUTPUT TABLE

The Output lookup table determines the 3-bit output of a given state and an interval in the joint cumulative distribution. The most-significant-bit (MSB) of the output is added to the incoming data stream and all three bits are returned to the decoder.

4.1.5 RANDOM NUMBER GENERATORS

Two random number generators produce 20 bits of random address for the State and Region lookup tables. Two generators of 63 and 64 stages, respectively, are used to increase the randomness of the addresses.

4.2 DETAILED CIRCUIT DESCRIPTION

The circuitry described in the following paragraphs is shown in the schematics in section 6.

4.2.1 CLOCKS

The TPG runs off two separate clocks: an internal clock generated by Schmitt-trigger oscillator U001 and an external clock that arrives with the data via line receiver J201. The internal clock ICLOCK is the clock used for communication with the HP9825, including handshaking, input registers and RAM loading. The data clock DCLOCK is used for the data path, including all pipeline registers and random-number-generators.

4.2.2 INPUT DATA FROM CALCULATOR

Data arrives from the HP9825 via input registers U102 and U103. The calculator's preset signal is used as a reset to initialize the card for loading. Handshaking is accomplished with J-K flip-

flop U101. A PCTL from the HP9825, indicating "data available" sets PFLG indicating "peripheral busy." Handshake signals and write-enables are generated from PFLG by U202 and U301. The signal HDSK1 is a pulse two clocks wide used to increment the address counters. The signal HDSK2 is one clock wide used to reset PFLG. A double pulse $\overline{WE1}$ is used as a write-enable to the RAMs that use both upper and lower bytes of input data. Signal $\overline{WE2}$ is a single write-enable to the RAMs that uses only the lower byte of of input data. The other line of communication with the HP9825 is CTL0. This is the GO signal to start the test set when loading is completed.

4.2.3 LOADING ADDESS COUNTERS

Loading address counters U402-U405 are enabled by the two clock wide HDSK1 which increments the counter twice on each transfer from the HP9825. The lower 13 bits of these counters are used to address the RAMs. The next two bits are decoded into chip-selects by decoder U401. Address lines are buffered by 3S buffers U501-U505. These buffers are also enabled by the sequencing decoder U401. When the load is completed, the Done signal is generated, resetting the load flip-flop.

4.2.4 RANDOM NUMBER GENERATORS

Random Number Generator (RNG) 1 consists of 64 stages using the polynomial $1+X+X^3+X^4+X^{64}$. It is shifted 16 times per DCLOCK (actually eight times on a clock at twice the frequency of DCLOCK). It provides seven bits to the Region array and five bits to the State array. Random Number Generator 1 consists of registers U106-U108, U207-U210, U311 and exclusive-OR gates U305-

U309. Random Number Generator 2 is a 63 stage RNG using polynomial $1+X+X^{63}$, shifted nine times per clock. It provides three bits of address to the State array and five bits to the Region array. Integrated circuits for RNG2 consist of U708, U709, U808, U809, U908, U909, U008, U009 and exclusive-OR gates U017-U019. The reset signal forces a "one" into both RNGs to ensure that they will not lock up with all zeros. The output of the RNGs are buffered by 3S registers U606-U608, enabled by GO.

4.2.5 RAMS

Table 4-1 shows how the 24 4Kx1 RAMs are arranged.

Table 4-1. Arrangement of RAMs

RAM	Function	Arrangement	Integrated Circuits
A	Next State	8Kx5	U903, U904, U905, U005, U703, U704, U705, U803, U804, U805
B	Region	4Kx8	U006, U007, U706, U707, U806, U807, U906, U907
C	Output	8Kx3	U701, U702, U801, U802, U901, U902

4.2.5.1 RAM A - The Next State RAM is addressed by eight bits of the RNG and five bits of its last output. The least significant bit (LSB) of its address is decoded into its selection lines. This RAM's output goes directly to the Hold State RAM and to the output RAM via pipeline registers U604 and U605.

4.2.5.2 RAM B - The Region RAM is addressed by 12 bits of the

RNG. Its output goes to the Output RAM via pipeline registers U602 and U603.

4.2.5.3 RAM C - The Output RAM is addressed by the outputs of RAMs A and B. The LSB of its address is decoded into selection lines. The output goes to output register U202.

4.2.5.4 HOLD STATE - The Hold State circuit consists of RAM U508 and counters U409, U410. The RAM is addressed by RAM A. It is loaded after the three large RAMs and before the GO signal is sent. The lower eight bits of this RAM are loaded into the counters. The carry-out of the counter is used to generate Gate and Flag signals, the enables to the output registers of RAMs A and B. Gate action is on a carry-out allowing the next state to be loaded into its register. Flag is active on either a carry-out or the ninth bit of the RAM being set. Thus, when there is no carry-out the state is held; and if the ninth bit is not set, the output is held also. Input data is complimented.

4.2.5.5 DATA PATH - Incoming data is latched into register U202. The MSB of the output of RAM C is exclusive-ORed with the data stream and synchronized again by U202. The data is returned through multiplexer U601 and line driver U104 to the decoder/deinterleaver. When desired the entire card can be bypassed through an external channel. The external data and clock arrives at line receiver U105 and leaves through the multiplexer and line driver.

SECTION 5

MAINTENANCE INSTRUCTIONS

Maintenance instructions are provided in the following paragraphs for both preventive and corrective maintenance of the TPG.

5.1 MAINTENANCE

Preventive maintenance of the TPG consists of cleaning and inspection procedures.

5.1.1 CLEANING

Clean the TPG as necessary, based upon visual inspections. The following items are needed to clean the equipment:

1. Soft, lint-free cleaning cloth
2. Trichloroethane
3. Soft-bristle brush.

WARNING

> The fumes of trichloroethane are toxic. Provide thorough ventilation whenever used. DO NOT USE NEAR AN OPEN FLAME. Trichloroethane is not flammable, but exposure of the fumes to an open flame or hot metal forms toxic phosgene gas.

Perform cleaning procedures, as follows:

1. Clean surfaces with a clean, soft, lint-free cloth.
2. Clean surfaces around switch annd indicator with a soft brush.

3. Clean painted surfaces with a cloth moistened in warm soapy water, if necessary.

4. To remove grease, fungus, or corrosion, use a cloth dampened in trichloroethane.

5.1.2 INSPECTION

To ensure that the TPG is always ready for operation, it should be inspected so that defects may be discovered and corrected before they result in serious damage or failure. The recommended preventive maintenance inspection procedures to be performed are listed in table 5-1. Other defects discovered during operation of the unit should be noted for future correction as soon as operation has ceased. Stop operation immediately if a deficiency is noted during operation which would damage the equipment.

Table 5-1. Maintenance Inspection

Item to be Inspected	Procedure	Schedule
Cabinet	Check TPG cabinet for cleanliness.	Monthly
Switch and Indicator	Check the mechanical action of the switch for smoothness and proper action.	Monthly
	Check the switch and indicator for proper action.	
Cables and Connectors	Check all interconnected cables and connectors for cracks and breaks. Tighten all connectors.	Monthly

5.2 CORRECTIVE MAINTENANCE

5.2.1 TROUBLESHOOTING

When there is no output from the TPG check the following first:

1. Loss of Internal Clock - The LOADTEST program can hang up while attempting to load the TPG RAMs. The symptom will be that the calculator display "Loading RAM 1" does not change.

2. Loss of External Clock - The loss of external clock will stop the RNGs. No data will go through the TPG.

3. Loss of Random Number Generators - Data will go through the TPG but the quality bits will be stuck at 11. Restart the RNGs by depressing special function key f2 (START). This may occur after a loss of the external clock.

5.2.2 PERFORMANCE VERIFICATION

To verify proper performance of the TPG, perform the following steps:

1. Load the TPG with a known good single-state distribution.

2. Connect a logic analyzer to the following points:

   a. U305-1 SIGN

   b. U202-6 MSB

   c. U202-4 LSB

   d. U202-9 CLOCK

3. Confirm that the relative frequency of each of the eight possible outputs is close to its expected value.

5.2.3 TROUBLESHOOTING AIDS

The following information is included to aid in troubleshooting the TPG.

The quality of the probability distributions may be observed by grounding J2-7. This will cause the test set to stay in the state it is in until J2-7 is ungrounded.

To cause the address counters to cycle without writing into RAMs, depress RESET on the calculator to go into LOAD mode and then ground J2-5.

To check the decoder/deinterleaver, incoming data can be forced to have two types of errors. Setting switch S2 located inside the front panel will cause the data to be delayed by one clock. Setting switch S3, also inside the front panel, will cause the incoming data to be inverted.

5.2.4 PLUG-IN CIRCUIT CARD ASSEMBLY (CCA) REPLACEMENT

To replace plug-in CCA proceed as follows:

1. Release the two front panel fasteners and lower the panel.
2. Lower nylon CCA retainer.

CAUTION

To avoid damage to circuit card ejectors, push ejectors back into place after ejecting the card from its receptacle; then pull the circuit card out of the enclosure.

3. Unseat the circuit card from the receptacle by first pulling outward on the circuit card ejector tabs. After unseating the circuit card, return the ejectors to their original position.

CAUTION

Exercise great caution when pulling out and inserting the card not to exert any pressure that would bend the card even a slight amount. Any bend from straight may cause damage to the circuit card.

4. Carefully pull the circuit card straight out of the chassis.

5. Lay the card on a clean, smooth-surfaced workbench with the component side up. Handle the card at the edges.

CAUTION

If an obstruction is felt when inserting a circuit card, remove the circuit card and determine the cause. Once the card is properly inserted, firmly exert equal force on both ejectors to make certain the card is correctly seated. Up to 48 pounds of force is required to securely seat the cards.

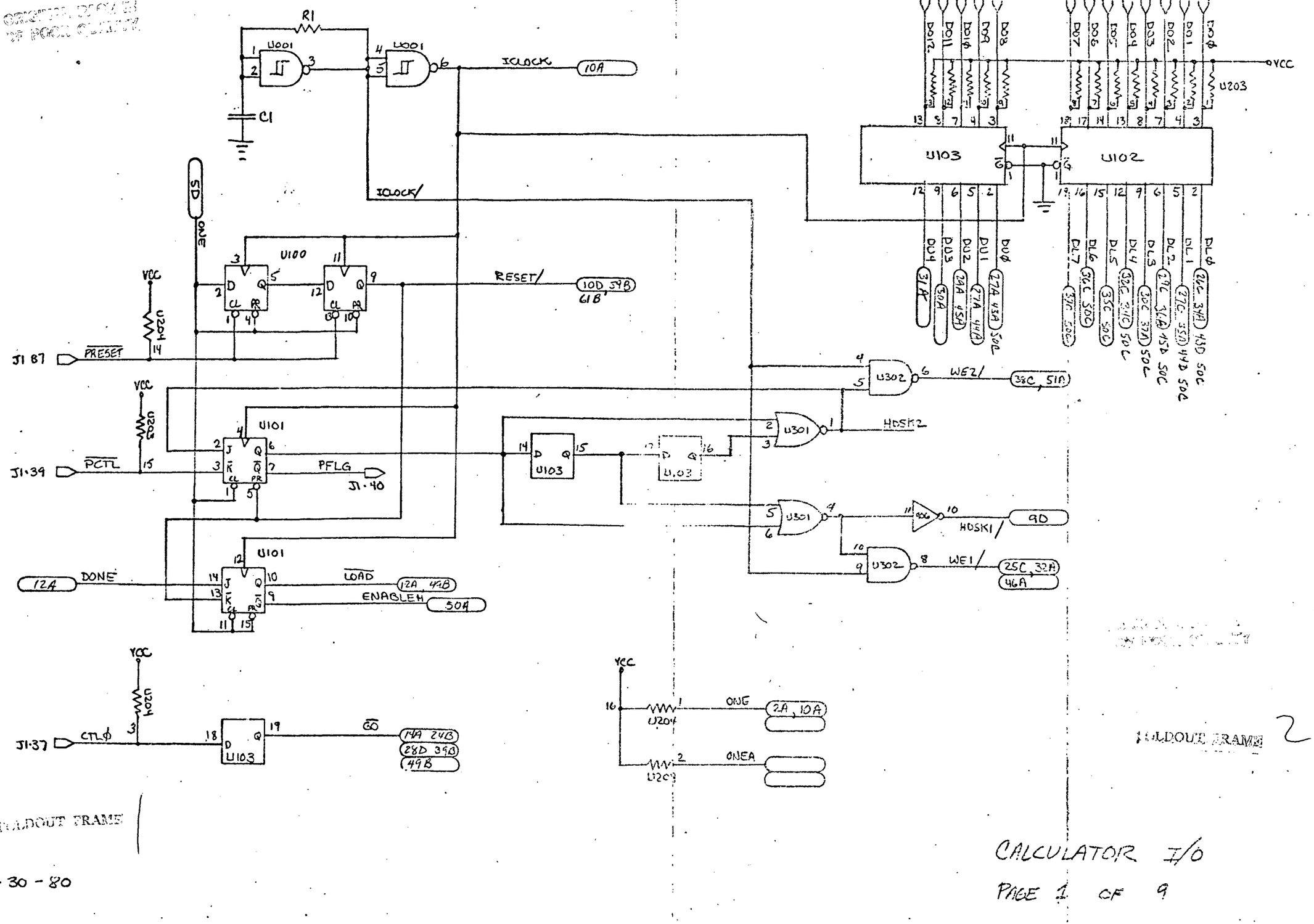
6. Insert the replacement circuit card assembly in the guide slots (component side up), and carefully press straight in until its connector is fully engaged in the receptacle. Fasten card retainer. Secure the front panel fasterners.

SECTION 6

LOGIC DIAGRAMS

The following logic diagram is contained in this section:

CALCULATOR I/O



PALDOUT FRAME

PALDOUT FRAME 2

10-30-80

CALCULATOR I/O

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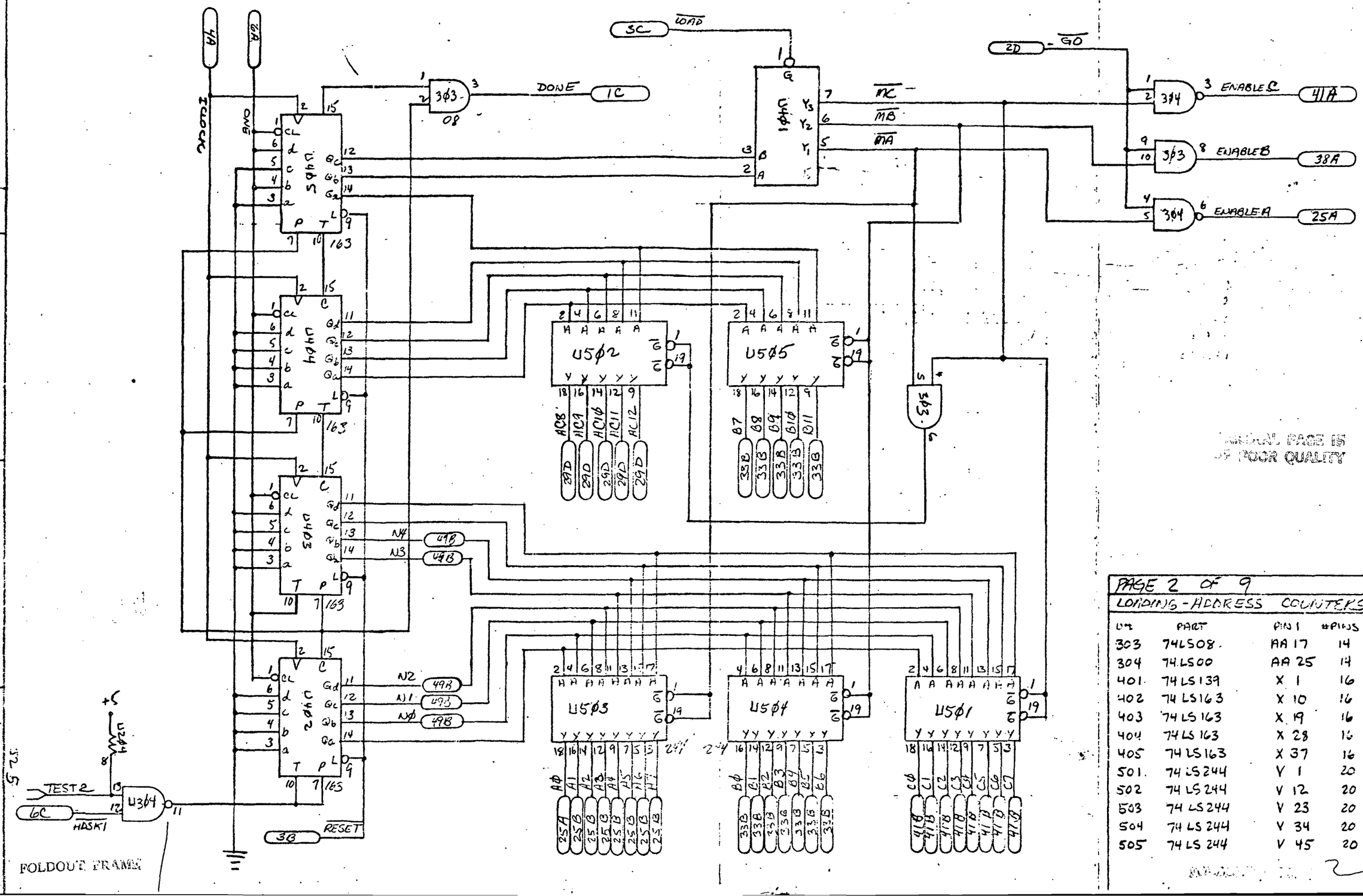

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LOADING - ADDRESS COUNTERS

U#	PART	PIN 1	#PINS	VCC	GND
303	74LS08	AA 17	14	14	7
304	74LS00	AA 25	14	14	7
401	74LS139	X 1	16	16	8
402	74LS163	X 10	16	16	8
403	74LS163	X 19	16	16	8
404	74LS163	X 28	16	16	8
405	74LS163	X 37	16	16	8
501	74LS244	V 1	20	20	10
502	74LS244	V 12	20	20	10
503	74LS244	V 23	20	20	10
504	74LS244	V 34	20	20	10
505	74LS244	V 45	20	20	10

74LS377

U209 U211 U210 U107 U207 U106 U108 U208

R7 R16 R4 R2 R19 R18 R13 R0 R5 R10 R14 R8

U304 74S00 U406 74S04 DRESET 63C

U306 U308 U308 U308 U307 U307 U307 U307 U308 U309 U306 U305 U309 U306 U309 U306 U305 74S86

DCLOCK1

U310

RDL-54-032

RNG1

$1 + x + x^3 + x^4 + x^{64}$

#1 RANDOM NUMBER GENERATOR

REVISION: 9-80

U008 U908 U808 U009 U909 U809 U709 U708

R1 R11 R7 R6 R9 R12 R5 R3

U018 U017 U016 U006

DRESET

DCLOCK2

REVISION:
9-80

U606 U607 U608

R19 R18 R17 R16 R15 R14 R13 R12 — A7 A6 A5 A4 A3 A2 A1 A0 — 25B 25B 25B 25B 25B 25B 25B 25A

R11 R10 R9 R8 R7 R6 R5 R4 — B11 B10 B9 B8 B7 B6 B5 B4 — 33B

R3 R2 R1 R0 — B3 B2 B1 B0 — 33B 33B 33B 33B

600 DCLOCK1 — GO 3D

— RNG2 —
$1 + x + x^{63}$

#2 RANDOM NUMBER GENERATOR

A B C D

ENABLE A

16A

4φ7 4φ6 4φ7

12D,24A Aφ

12D,24A A1 A2 A3 A4 A5 A6 A7

HC8 HC9 HC10 HC11 HC12

DUφ 8B DU1 DU2 DU3 DU4

WE1 6C

U9φ4 U7φ5 U8φ5 U9φ5 Uφφ5

U7φ3 U8φ3 U9φ3 U7φ4 U8φ4

DLφ DL1 DL2 DL3 DL4

8A 50B 7φ T1 T2 T3 T4 29D,50B

U6φ4 U6φ5

54B GATE 60D CLOCK1 3D 6Q 32C T4

A08 HC9 HC10 HC11 HC12 12B,41B 12C,41B

FOLDOUT FRAME

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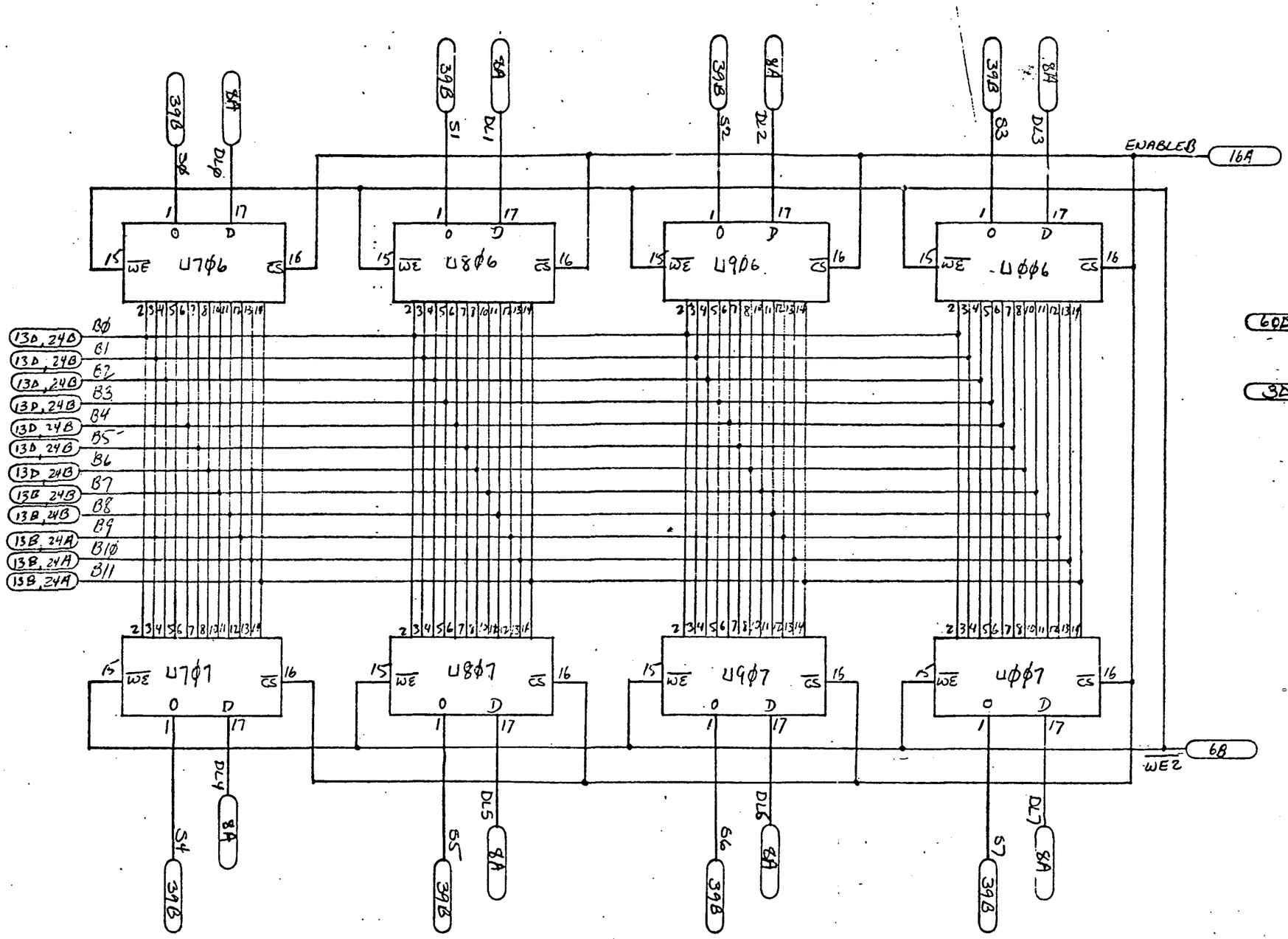
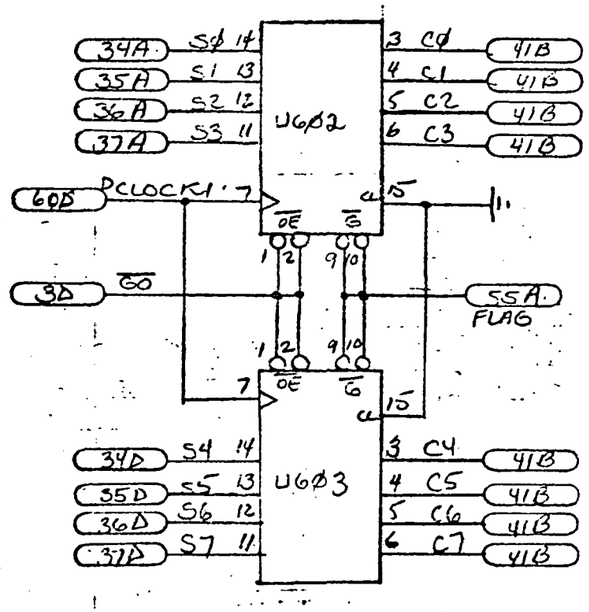
8K x 5 STATE MEMORY A

U#	PART	PIN 1	#PINS	VCC	GND
406	74LS04	X 46	14	14	7
407	74LS00	X 54	14	14	7
604	74LS173	T 28	16	16	8
703	93471	R 21	18	18	9
704	93471	R 31	18	18	9
705	93471	R 41	18	18	9
803	93471	P 21	18	18	9
804	93471	P 31	18	18	9
805	93471	P 41	18	18	9
903	93471	M 21	18	18	9
904	93471	M 31	18	18	9
905	93471	M 41	18	18	9
005	93471	K 41	18	18	9
605	74LS173	T 37	16	16	8





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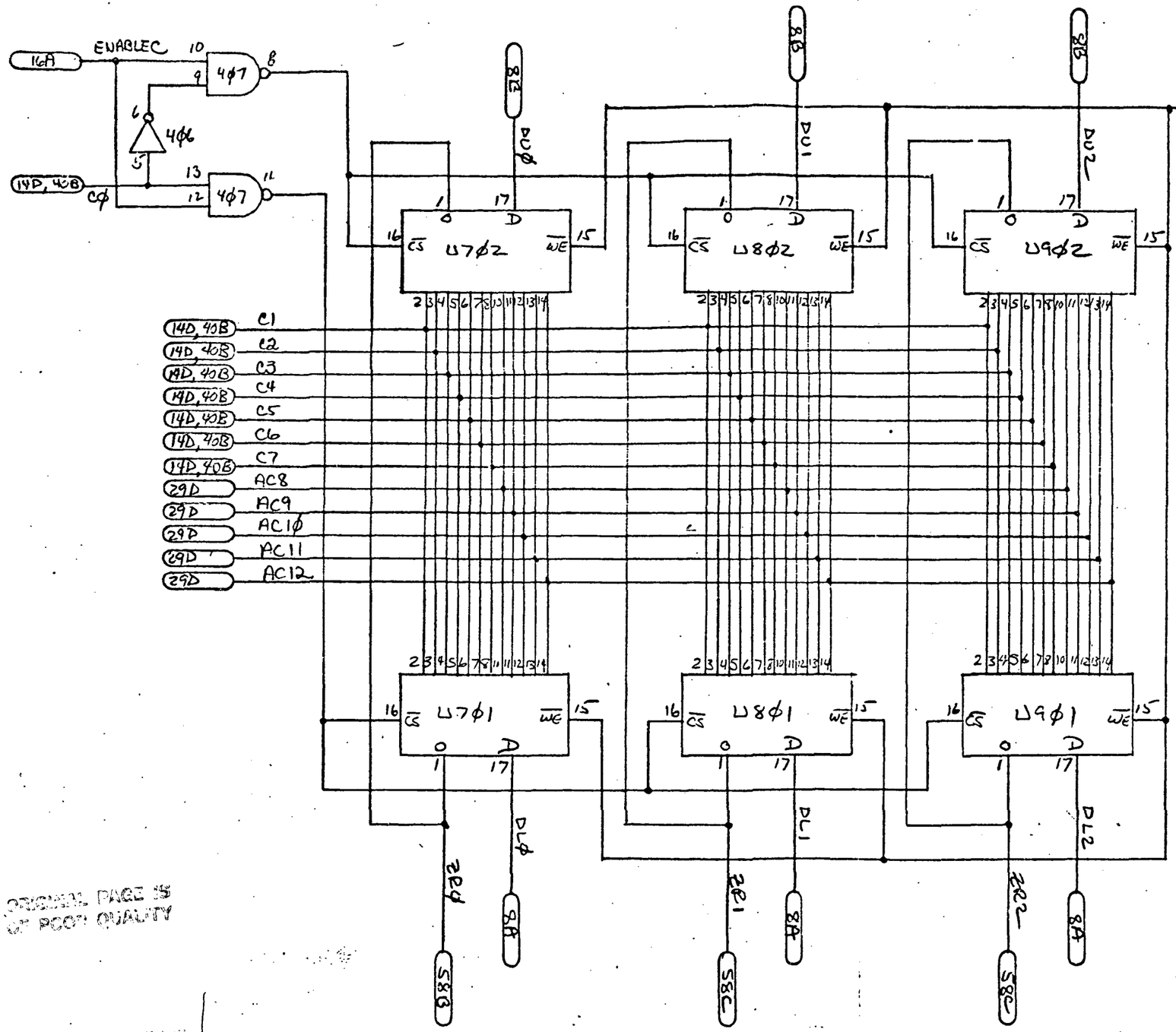
4K x 8 "REGION" MEMORY B

U#	PART	PIN 1	#PINS	VCC	GND
602	74LS173	T10	16	16	8
706	93471	R51	18	18	9
707	93471	R61	18	18	9
806	93471	P51	18	18	9
807	93471	P61	18	18	9
906	93471	M51	18	18	9
907	93471	M61	18	18	9
006	93471	K51	18	18	9
007	93471	K61	18	18	9
603	74LS173	T19	16	16	8



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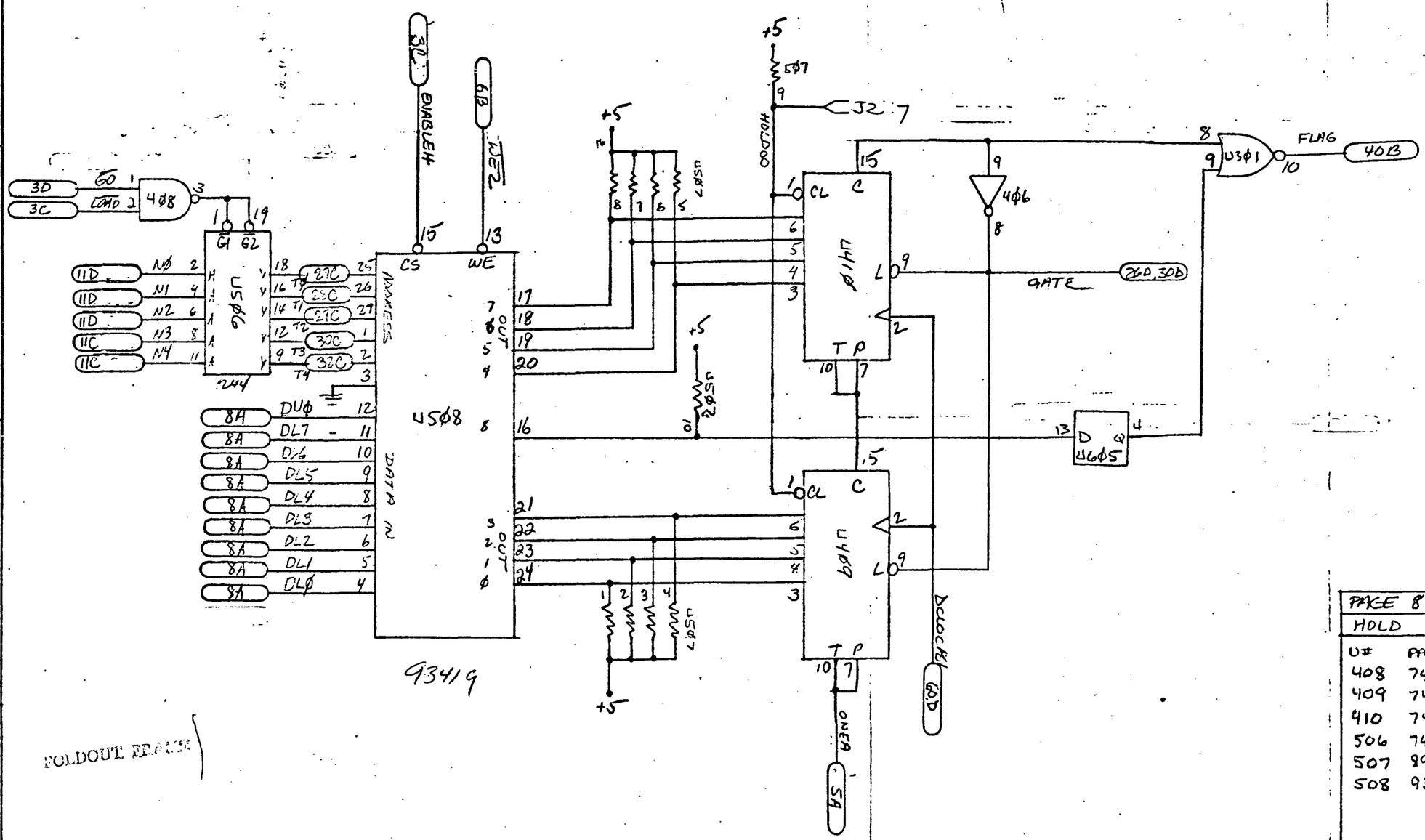
8K x 3 OUTPUT MEMORY C

U#	PART	PIN1	#PINS	VCC	GND
7φ1	93471	R 1	18	18	9
7φ2	93471	R 11	18	18	9
8φ1	93471	P 1	18	18	9
8φ2	93471	P 11	18	18	9
9φ1	93471	M 1	18	18	9
9φ2	93471	M 11	18	18	9



FOLDOUT FRAME

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HOLD STATE					
U#	PART	PIN 1	#PINS	VCC	GND
408	74LS00	X 62	14	14	7
409	74LS163	X 70	16	16	8
410	74LS163	X 79	16	16	8
506	74LS244	V 56	20	20	10
507	898-1-RIK	V 67	16	16	—
508	93419	V 79	28	28	14

A

B

C

D

U105

CLKINT
CLKINF
IN0T
IN0F
IN1T
IN1F
IN2T
IN2F

J2·2 (B1) BYPASS

+5

U601

U601

U104

CLKOUTT
CLKOUTF
1OUTT
1OUTF
2OUTT
2OUTF
3OUTT
3OUTF

43 RESET/

43D 2R0
44D 2R1
45D 2R2

5D ONEA

U206

U305

U305

U406

U202

U202

DRESET RNG1, 2

FOLDOUT FRAME

U201

INT
INF
CLKT
CLKF

U202

U302

U302

DCLOCK1 28D 39B 53D, RNG1, 22B

DCLOCK2 RNG2

BITSLIP

INVERT

U000

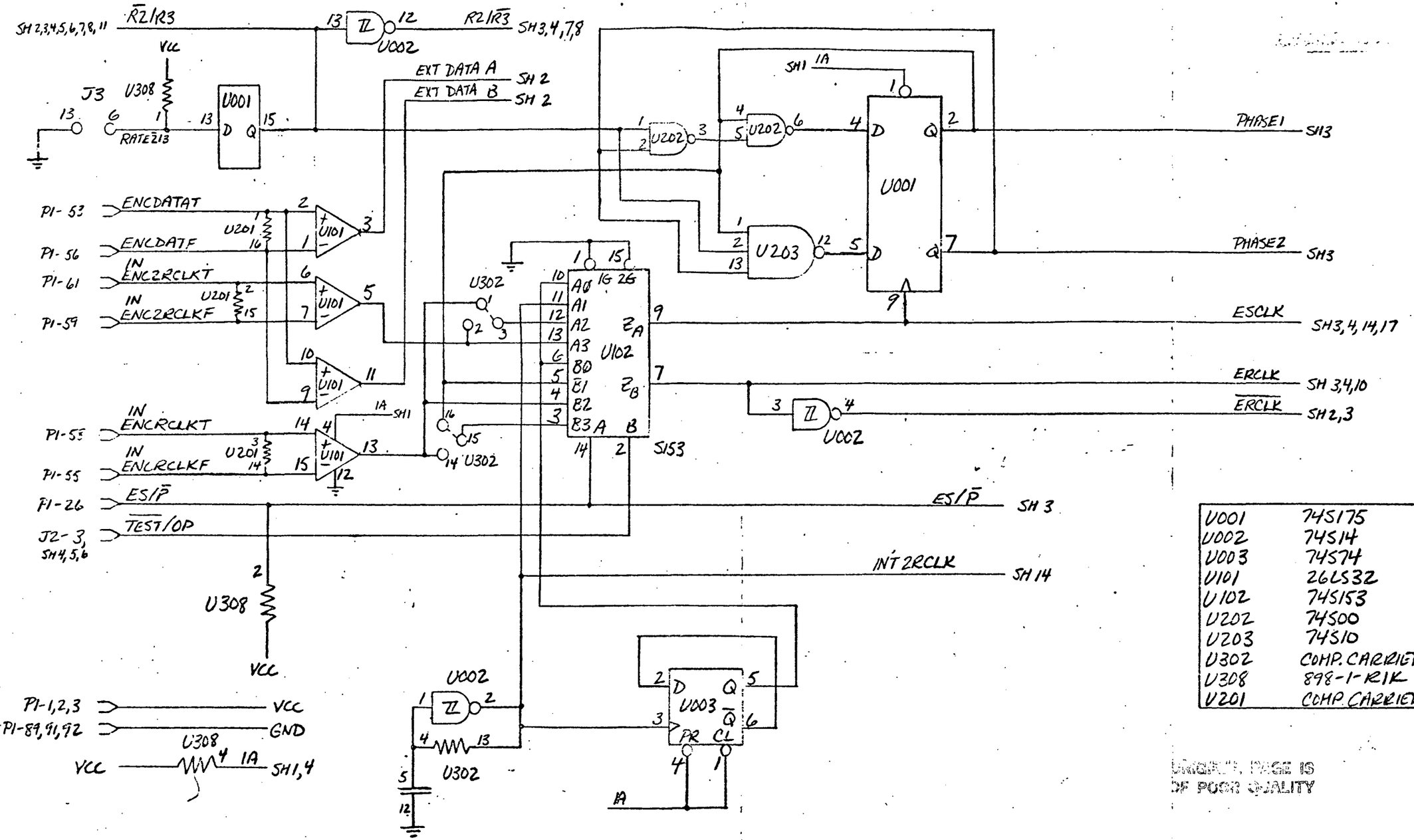
R2 R3 (S2)

R4 R5 (S3)

NC NO C

DATA PATH
PAGE 9 OF 9

11-3-80



U001	74S175
U002	74S14
U003	74S74
U101	26LS32
U102	74S153
U202	74S00
U203	74S10
U302	COMP. CARRIER
U308	898-1-R1K
U201	COMP. CARRIER

I10 BOARD	LD21368	SH1
ENCODER CLOCKS		

U004	825129
U005	825129
U006	74LS174
U103	74LS157
U104	74LS164
U105	74LS164
U204	74LS08
U205	74LS86
U206	74LS27
U207	74LS86
U308	898-1-R1K
U911	COMP. CARRIER
U912	96L02

SH2 1B

SH10 INT DATA

SH1 EXT DATA A

SH1 EXT DATA B

J2-1 DATA INT/EXT

U103

U308

VCC

U104

U105

U004

U005

U006

U205

U204

ERCLK

ENC DIFF

J3 2 17

U510

J3 18 1 REVERSE

PA SH3

PB SH3

PC SH3

U205 U205 U207

U206

FOLDOUT FRAME 2

ORIGINAL PAGE IS OF POOR QUALITY

U912

ENC FLT J2-4

U911

VCC U308 5 1B SH2,3

FOLDOUT FRAME 1

ORIGINAL PAGE IS OF POOR QUALITY

I/O BOARD SH 2

ENCODER

SH1 $\overline{ERCLK}$ 12 — U202 — S00 — 11

SH1 R2/$\overline{R3}$ 13 — U202

SH1 $\overline{R2}$/R3 9 — U202 — S00 — 8

10 — U202

(REGISTER U001 CLOCKED BY ESCLK)

U001: 12 D, 11 $\overline{Q}$

1, 2 — U208 — S00 — 3

SH1 ES/$\overline{P}$ 4

ENC INV 5 — U208 — 6

3, 2 — U108 — S02 — 1

9 U308 — VCC

5, 4 — U207 — 6

9, 10 — U207 — 8

J3: 16, 3

LS153

SH2 PC 6

SH2 PA 3

SH2 PB 4

U106: Aϕ, A3, A2, 1G, 2G, B, A; 4A = 7

1G = 1, 2G = 15

SH1 PHASE2 2

SH1 PHASE1 9 — U208 — 8 — 10

SH1 ES/$\overline{P}$

SH2 1B

SH1 ESCLK

U107: 4 PR, 1 CL, 2 D, 3, 11, 12 D, 10 PR, 13 CL; Q 5, $\overline{Q}$ 6, $\overline{Q}$ 8, Q 9

SH2 1B — U401: 4, 2, 1, 3, 12

SH1 ERCLK

OUT ENCRCLKT — P1-52

OUT ENCRCLKF — P1-50

SH1 ESCLK — U401: 6, 7, 5

OUT ENC2RCLKT — P1-49

OUT ENC2RCLKF — P1-47

S74

U401: 10, 11

ENCIOUTT — P1-43

ENCIOUTF — P1-41

U401: 14, 13

ENCQOUTT — P1-44

ENCQOUTF — P1-46

PCA — SH14

PCB — SH14

U001	74S175
U106	74LS153
U107	74S74
U108	74S02
U202	74S00
U207	74LS86
U208	74S00
U308	898-1-R1K
U401	26LS31

IO BOARD SH 3

ENCODED DATA FORMATTING

U002	74S14
U203	74S10
U301	26LS32
U303	74S175
U304	74S37
U308	8T8-1-121K
U402	74128
U403	74S153
U509	74LS08
U704	74S157
U805	74LS00

SH1 1A

SH 1 R2/R3

U805

U304

U203

U303

INTCLK → P1-19

SH1 1A

P1-34 DEC2RCLKT
P1-32 DEC2RCLKF
P1-29 DECRCLKT
P1-31 DECRCLKF

U201 4 13
U201 5 12

U301

S153

U403

U704

U304 S37

DSCLK → SH6
DSCLK → SH5
DRCLK → SH6,7,8,11,12,14,17
DRCLK → SH6, 9,11,12,13
P1-68

LS128

U402

DRCLK1 → SH9

SH1,3,14 ESCLK
SH 1,10 ERCLK
SH1, J2-3 TEST/OP
P1-28 DS/P

SH8 INTLVR IN

U002

SERIPAR SH16,5

U308

Vcc

SH1 R2/R3

U509

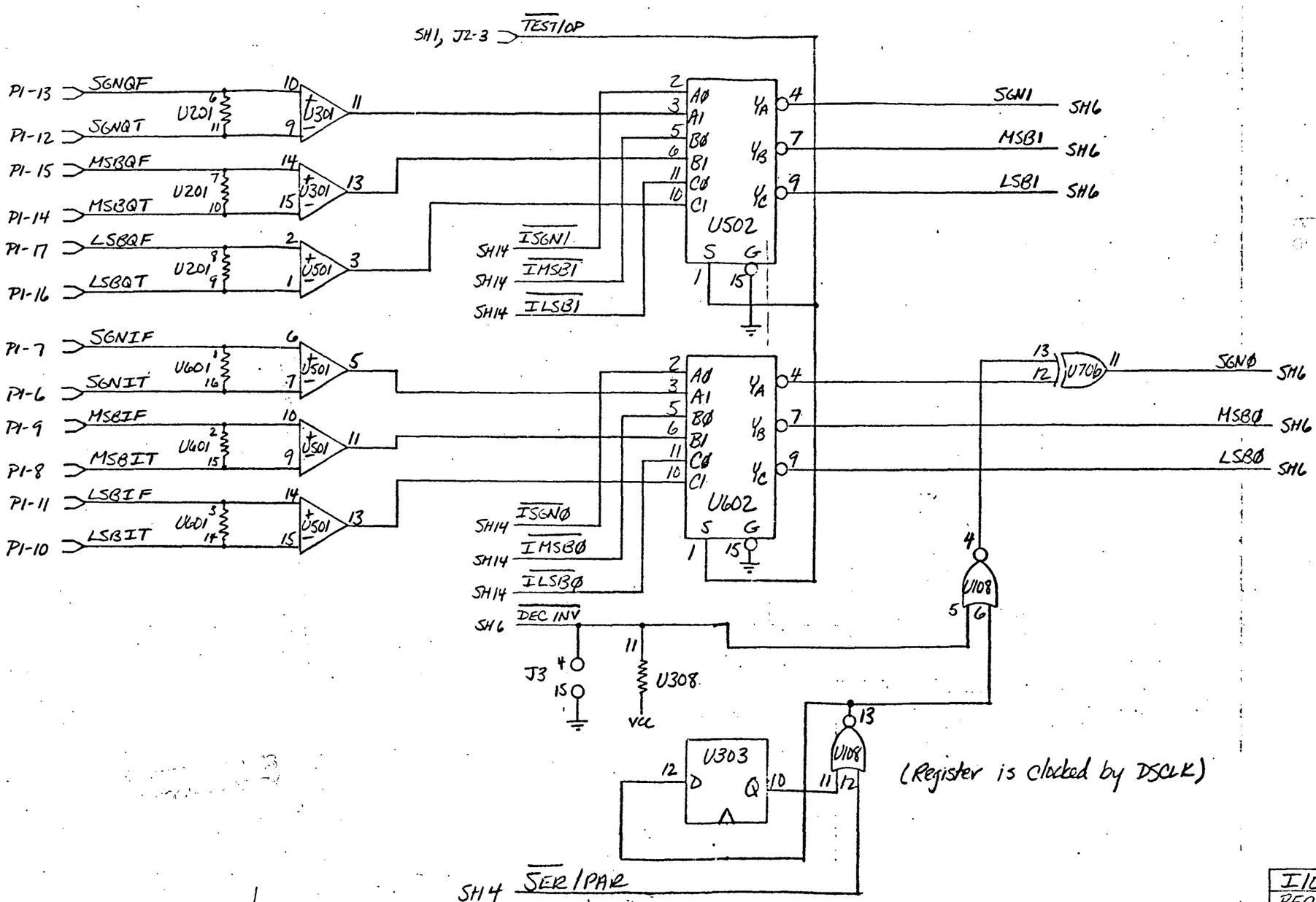
R2SYNC → SH6

FOLDOUT FRAME

FOLDOUT FRAME

I/O BOARD SH 4
DECODER CLOCKS

L. 1108	74S02
L 1301	26LS32
L 1303	74S175
L 1308	898-1-R1K
L 1501	26LS32
L 1502	74LS158
L 1602	74LS158
L 1706	74LS86



FOLDOUT FRAME

FOLDOUT FRAME

I/O BOARD SH 5

RECIEVE INF JT SYMBOLS FOR DECODE

SH5

FOLDOUT FRAME

SH 4 $\overline{DSCLK}$

SH5 SGNØ

SH5 MSBØ

SH5 LSBØ

U503 (CP, DA, DB, DC, CL; QA, QB, QC)

U504 (AØ, AI, BØ, BI, CØ, CI, E; YA, YB, YC)

SH8 IE

SH8 SYNC2

SH1 $\overline{R2IR3}$

SH4 R2SYNC

U404

PI-25 OFQPSK/$\overline{QPSK}$

SH1, J2-3 $\overline{TEST/OP}$ 11

U302

U308

VCC

SH8 $\overline{HARD/SOFT}$

SH4 DRCLK

SH5 SGNI

SH5 MSBI

SH5 LSBI

U603 (CP, CLR, DA, DB, DC, DD; QA, QB, QC, QD)

U604 (AØ, AI, BØ, BI, CØ, CI, E; YA, YB, YC)

PI-79 NORM

NORMALIZE SH 8, 15, 17

SH 4 $\overline{SER/PAR}$

PI-67 DATA OUT

U405 (CLR, RS, A, B, C; QA, QB, QC, QD, SI, SØ)

U306

U505 (CLR, RS, A, B, C; QA, QB, QC, QD, SI, SØ)

U605 (CLR, RS, A, B, C; QA, QB, QC, QD, SI, SØ)

SH4 $\overline{DRCLK}$

U406 (AØ, AI, BØ, BI, CØ, CI, S; QA, QB, QC, QD)

U506 (AØ, AI, BØ, BI, CØ, CI, DØ, DI, S; QA, QB, QC, QD)

U606 (AØ, AI, BØ, BI, CØ, CI, DØ, DI, S; QA, QB, QC, QD)

SH1 $\overline{R2IR3}$

SH8 SYNC1

U109

SGNA SH6,12

MSBA SH6

U305 LSBA SH6

SGNB SH6,12

MSBB SH6

U305 LSBB SH6

DEC OUTPUT SH9,11

U307 SGNC SH7,12

MSBC SH7

U305 LSBC SH7

DEC OUT 1 SH9

U108	74S02
U302	COMP. CARRIER
U305	74LS86
U306	74LS04
U307	74LS08
U308	898-1-R1K
U404	74LS00
U405	74LS194
U406	74LS298

U503	74LS174
U504	74LS157
U505	74LS194
U506	74LS298
U603	74LS174

U604	74LS157
U605	74LS194
U606	74LS298

I/O BOARD SH6

DECODER NODE & PHASE SYNC

FOLDOUT FRAME

U304	74S37
U407	74S472
U408	74S472
U409	74S472
U507	74S472
U508	74S472
U511	74128
U607	74S472
U608	74LS377
U609	74LS377
U610	74LS377
U611	74128
U612	74128
U701	74128
U702	74128
U703	74128

I/O BOARD SH7
DECODER METRIC PROM

FOLDOUT FRAME

FOLDOUT FRAME

VCC — U308 — 13 IE SH8,6,7

VCC — U159 — 16 — 15 14 — 15 14

SH8 IE — 11 12 — U160 Q — 10 — SYNC — J2-5

13 — SYNC — SH9

SYNC1 — SH6

SYNC2 — SH6

U203 — 8 — 9 10 11

U706 — 4 5 — 6

U707 — 1 CL — 4 D — 2 Q — 9

U706 — 9 10 — 8

U804 — 14 13 — Q_A Q_B — 7 P — 10 T — 2 — CL A B C D LD — 1 3 4 5 6 9

U806 — 3 — 4

SH6,15 NORMALIZE

SH8 IE — 1 10 7 — CL T P — U152 — A B C D — C 15 10 T

SH8 IE — 1 7 — CL P — U802 — A B C D LD — C 15 1

U806 — 2

SH8 IE — 1 — U806 — 8

U509 — 6

4 3 2 6 7 — $\bar{E}$ Q_A Q_B Q_C Q_D — 5 $\bar{U10}$ — 14 LD — U803 — D3 — 9

11 — IE — SH8

INTLVR IN — SH4

U806 — 9

U509 — 4 5

U705 — 8 — 11 10 9

R2/R5 1 — 2 — U172 — 3 — 4 5 6 9 2

U172 — 4 5 — 6

4 — U510 — VCC

U172 — 11 — 12 13

U172 — 8 — 9 10

DRCLK — SH4

R2/R3 — SH1

DSCLK — SH4

9 — U503 — D Q — 13 — 12

PI-27 — HARD/SOFTIN

HARD/SFT SH6

TDMA — 14 — 15

PI-22

PI-24

14 15 — U308 — VCC

R2/R3 — SH11

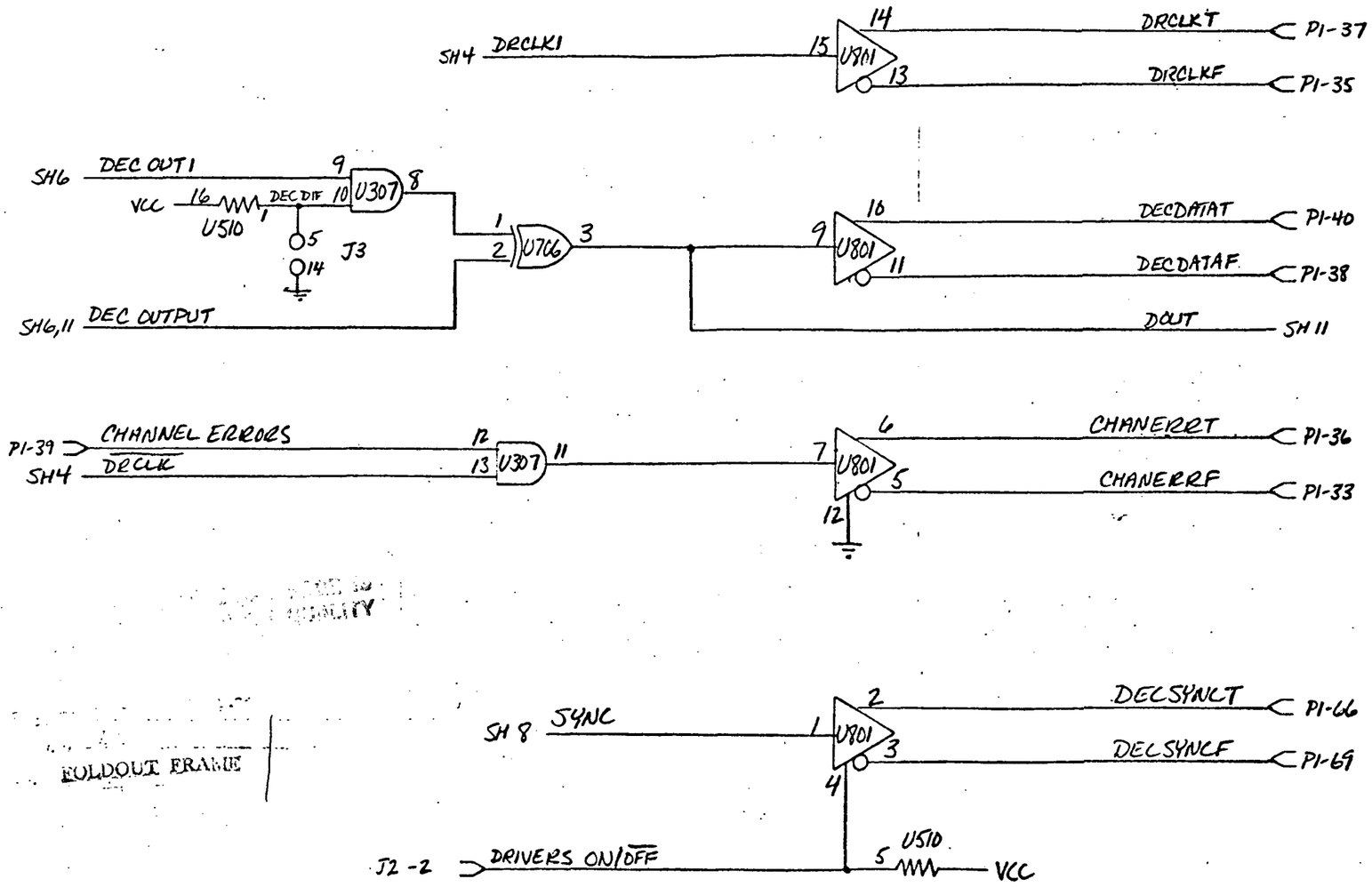
INTLVR IN — SH4

U203	74S10
U308	898-1-R2K
U503	74LS174
U509	74LS08
U705	74LS10
U706	74LS86
U707	74LS175
U802	74LS163
U803	74LS191
U804	74LS163
U806	74LS14
U152	74LS163
U159	COMP. CARRIER
U160	96L02
U172	74LS00

I/O BOARD — SH 8

DECODER SYNC LOSS DETECTION

JUMPER SELECTS NOT DIFFERENTIAL CODING WHEN TIED.

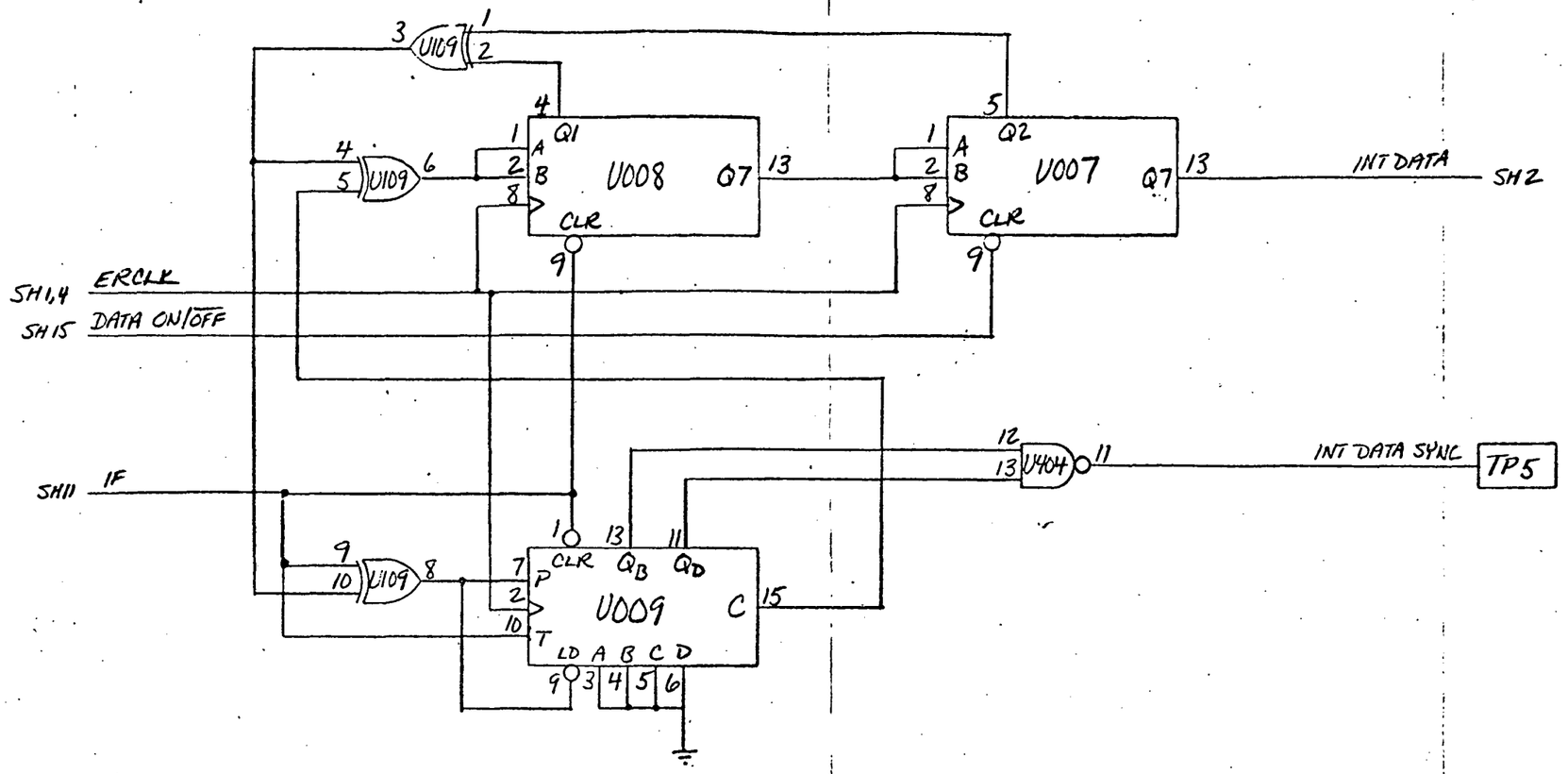


FOLDOUT FRAME

FOLDOUT FRAME

U307	74LS08
U510	898-1-R1K
U706	74LS86
U801	26LS31

I/O BOARD	SH9
DECODER OUTPUT & DIFF. DECODE	



U007	74LS164
U008	74LS164
U009	74LS163
U109	74LS86
U404	74LS00

I/O BOARD SH 10

ENCODER INTERNAL DATA GENERATION

U012	74LS157	U410	74LS74
U109	74LS86	U411	74LS163
U112	74LS00	U412	74LS163
U209	74LS86	U413	74LS153
U210	74LS86	U509	74LS08
U211	74LS164	U510	898-1-R1K
U212	82S129	U707	74LS175
U306	74LS04	U711	74LS04
U309	74LS51		
U310	74LS164		
U311	74LS164		
U313	74LS02		

SH4 DRCLK

SH12 DELAY OUTA

SH12 DELAY OUTB

SH12 DELAY OUTC

SH9 DECODER OUTPUT

SH11 IF

SH11 DOUT

SH4 DRCLK

SH1 $\overline{R2/R3}$

$\overline{DEC\ REV}$ SH7

VCC U510 J3

U211 U212 U209 U109 U306 U309 U310 U311 U312 U313 U410 U411 U412 U413 U509 U707 U711

CHANNEL ERROR SH13,17

OUTPUT ERROR SH13,15

MAX MIN DN/UP

VCC U510 2 IF SH 11,12,13

I/O BOARD SH 11

CHANNEL & OUTPUT ERROR MONITOR

U010	93L422
U011	93L422
U110	74LS163
U111	74LS163
U112	74LS00
U207	74LS86
U306	74LS04
U510	898-1-R1K
U707	74LS175

SH4 DRCLK
SH6 SGNA
SH6 SGNB
SH6 SGNC
U112
IF SH11
U010
U011
DELAY OUT A SH11
DELAY OUT B SH11
DELAY OUT C SH11
U110
U111
U207
U306
U707
SH4 DRCLK
SH11 IF
J3
PATH32
U711
VCC
U510

FOLDOUT FRAME

FOLDOUT FRAME 2

I/O BOARD SH12
ERROR MONITORING – P.M. DELAY COMPENSATION

Row 7

SH 11 IF

SH4 $\overline{DRCLK}$

J2-6 $\overline{CHAN/OUTP\ ERRORS}$

SH9,11, P1-39 CHANNEL ERROR

SH11,15, OUTPUT ERROR

J2-8 10^5

J2-11 $\overline{MAN/AUTO}$

J2-12 GATE

$\overline{CNTR1\ CLK}$ J2-9

AUTO GATE J2-13

$\overline{CNTR2\ CLK}$ J2-10

$\overline{CNTR2\ CLR}$ J2-7

CNTR2 LD J2-17

U708 U709 U710 U711 U712 U713 U714 U806 U807 U808 U809 U810

U708	74LS157
U709	74LS160
U710	74LS160
U711	74LS04
U712	74LS00
U713	COMP CARRIER
U714	96L02
U806	74LS14
U807	74LS160
U808	74LS160
U809	74LS160
U810	74LS160

BOLDOUT FRAME

I/O BOARD SH13

ERROR STATISTICS COUNTER

U014	74LS164
U112	74LS00
U113	74LS164
U114	74LS164
U115	74LS164
U210	74LS86
U213	74LS161
U214	82S129
U215	74LS174
U314	74LS86
U315	74LS298

SH15 NOISE ON/OFF

SH1 INT 2RCLK

SH4 DRCLK

SH8 IE

SH15 SGN ON/OFF

SH1 ESCLK

U014 U115 U114 U113 U213 U214 U215 U315 U210 U314 U806 U112

ISGNØ IMSBØ ILSBØ ISGNI IMSBI ILSBI — SH5

P0A P0B — SH3

IE — SH8

I/O BOARD SH14

CHANNEL NOISE SIMULATOR

SH11,13 OUTPUT ERRORS

SH6,8 NORMALIZE
SH 15 ENORM

J2-34 START

U901 .330 3.3MF U601

U153 U154 U155 U173 U174 U175 U905 U906 U907 U908 U712 U313 U314 U208 U711 U901 U961

FLT SH7

FLT BD1 J2-16
FLT BD2 J2-14
FLT BD3 J2-15
EMUX SH16
S1 SH16
S2 SH16

D0 SH16
D1 SH16
D2 SH16
D3 SH16

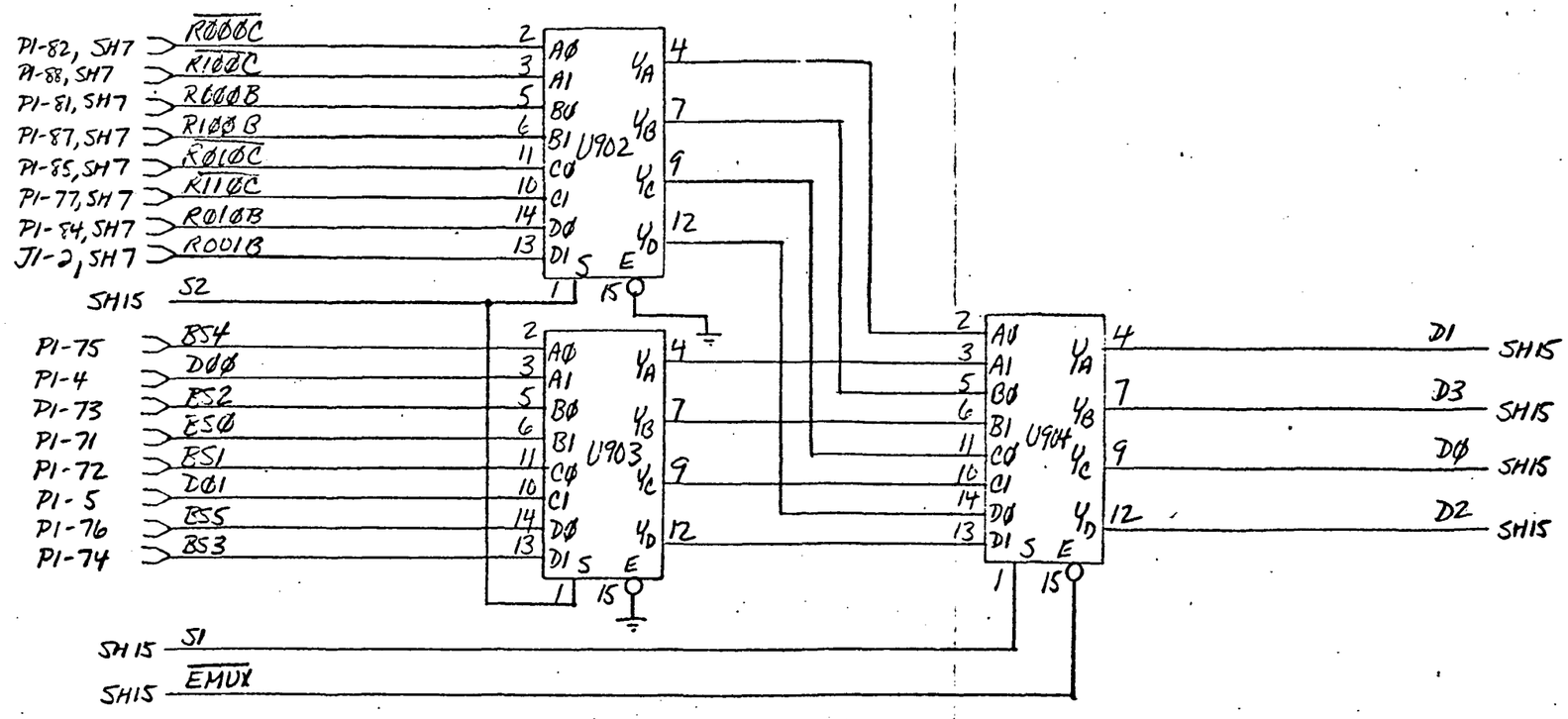
DATA ON/OFF SH10
ENDEH SH15
SGN ON/OFF SH14
NOISE ON/OFF SH14

FOLDOUT FRAME

U208	74S00	U907	74LS138
U313	74LS02	U908	74LS02
U314	74LS86	U153	74LS163
U601	COMP. CARRIER	U154	82S123
U711	74LS04	U155	74LS04
U712	74LS00	U173	74LS163
U901	74LS132	U174	82S123
U905	74100	U175	74100
U906	74100	U176	96L24

I10 BOARD SH15
BUILT-IN-TEST

U902	74LS157
U903	74LS157
U904	74LS157



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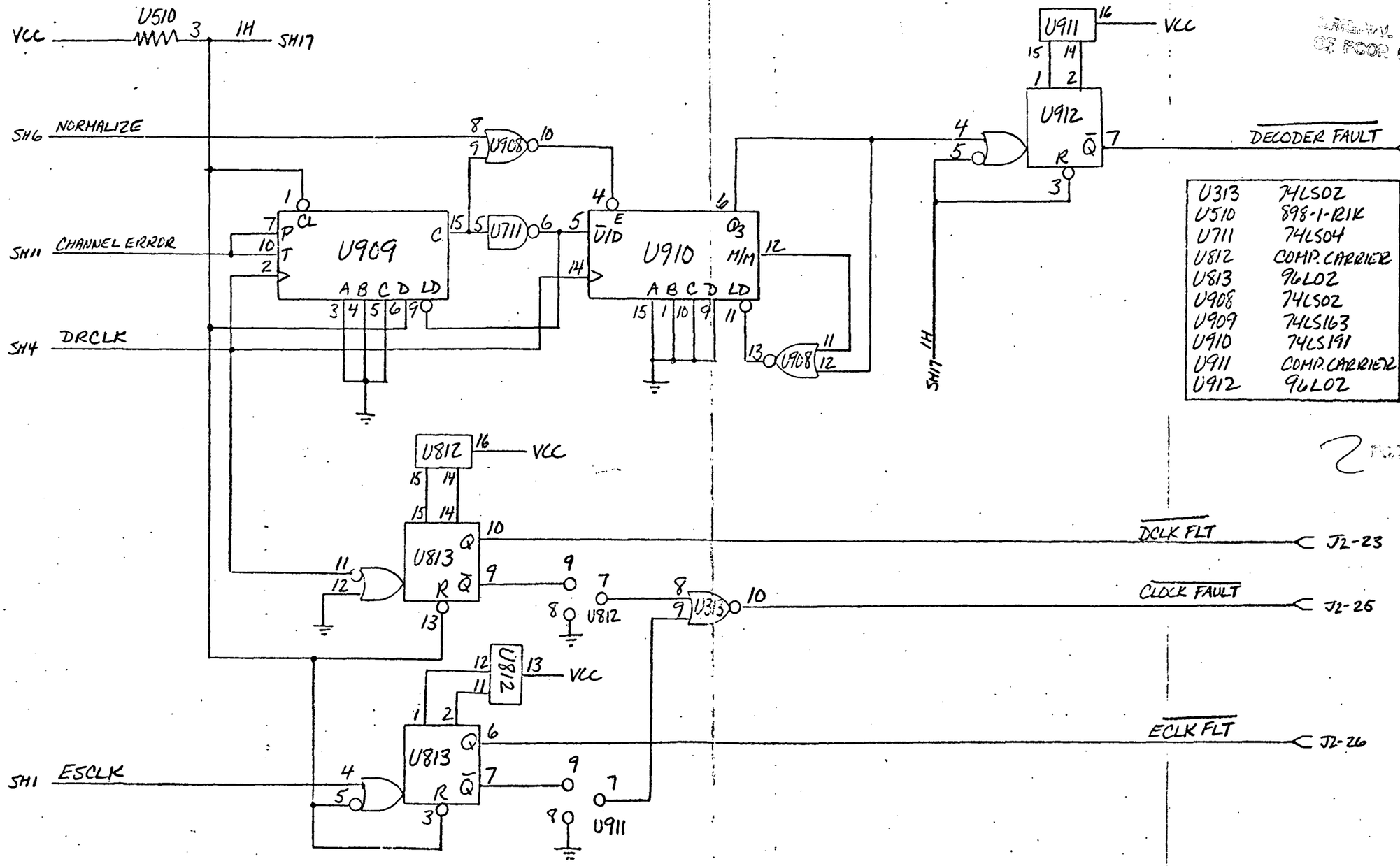
FOLDOUT FRAME

FOLDOUT FRAME 2

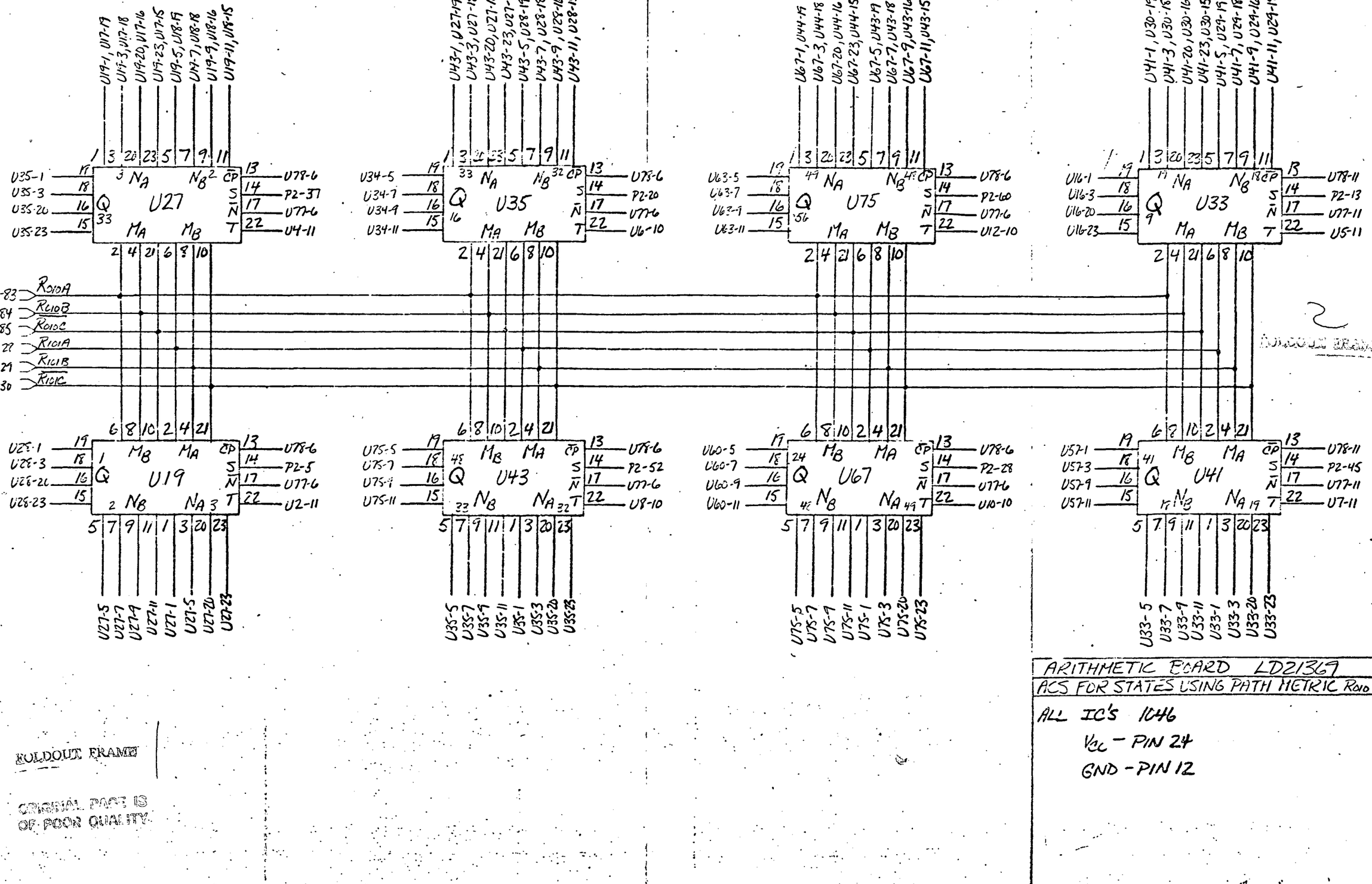
I10 BOARD	SH16
BUILT-IN-TEST	



U313	74LS02
U510	898-1-121K
U711	74LS04
U812	COMP. CARRIER
U813	96L02
U908	74LS02
U909	74LS163
U910	74LS191
U911	COMP. CARRIER
U912	96L02

I/O BOARD SH 17

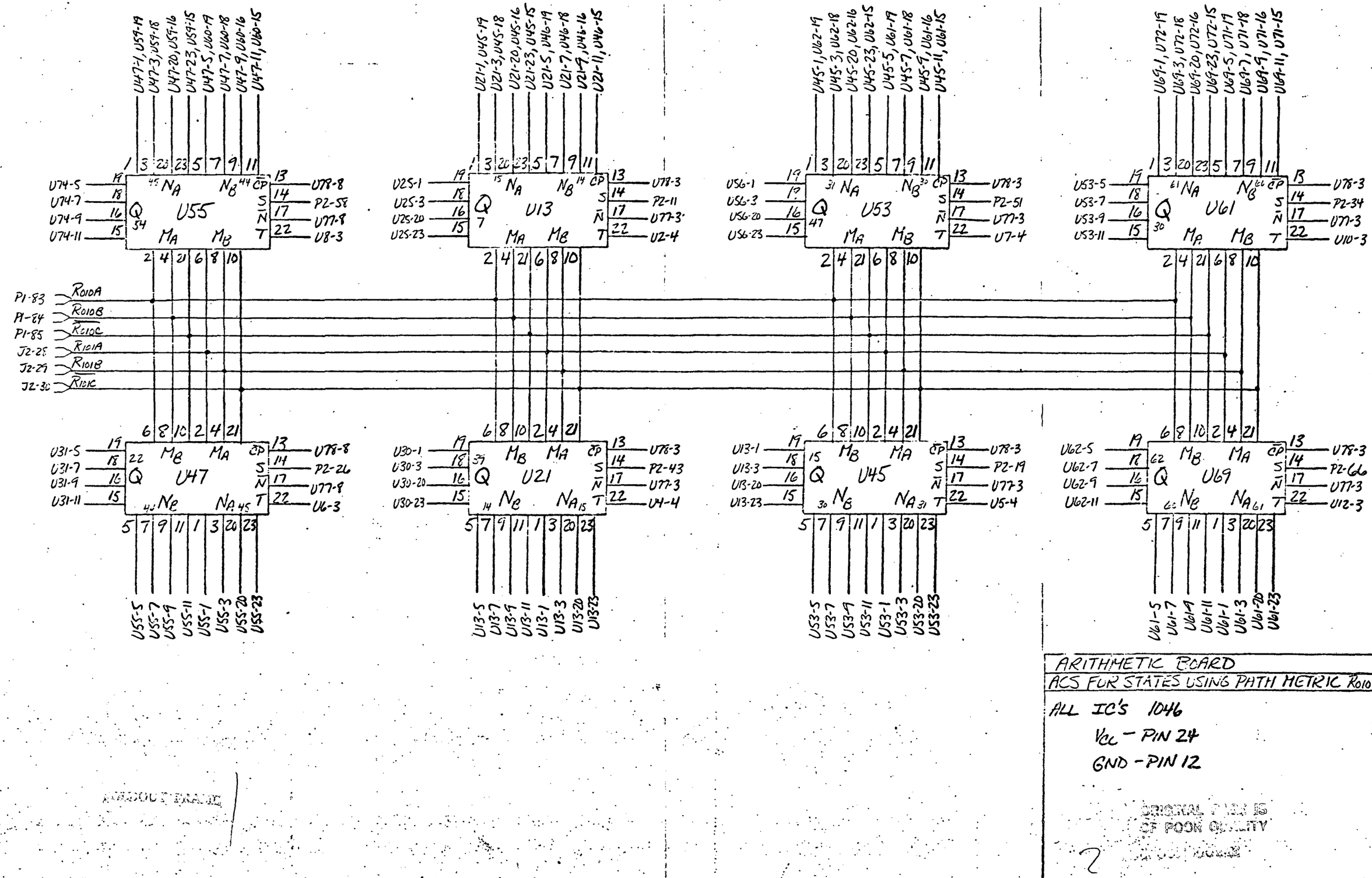
BUILT-IN-TEST FAULT SIGNALS



ARITHMETIC BOARD LD21369
ACS FOR STATES USING PATH METRIC R010

ALL IC'S 1046
V_{CC} - PIN 24
GND - PIN 12

FOLDOUT FRAME



ARITHMETIC BOARD
ACS FOR STATES USING PATH METRIC R010

ALL IC's 1046
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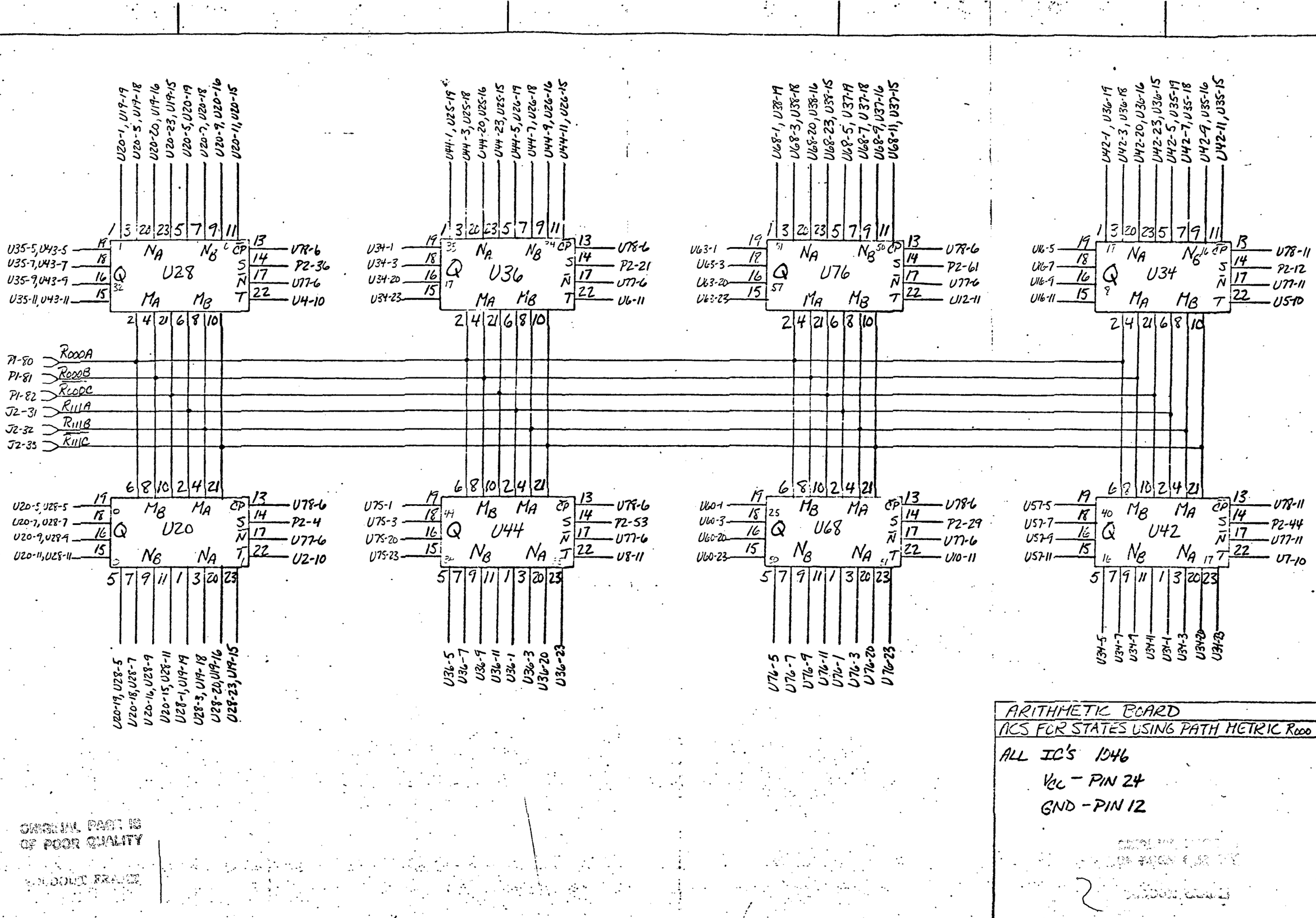
GND - PIN 12



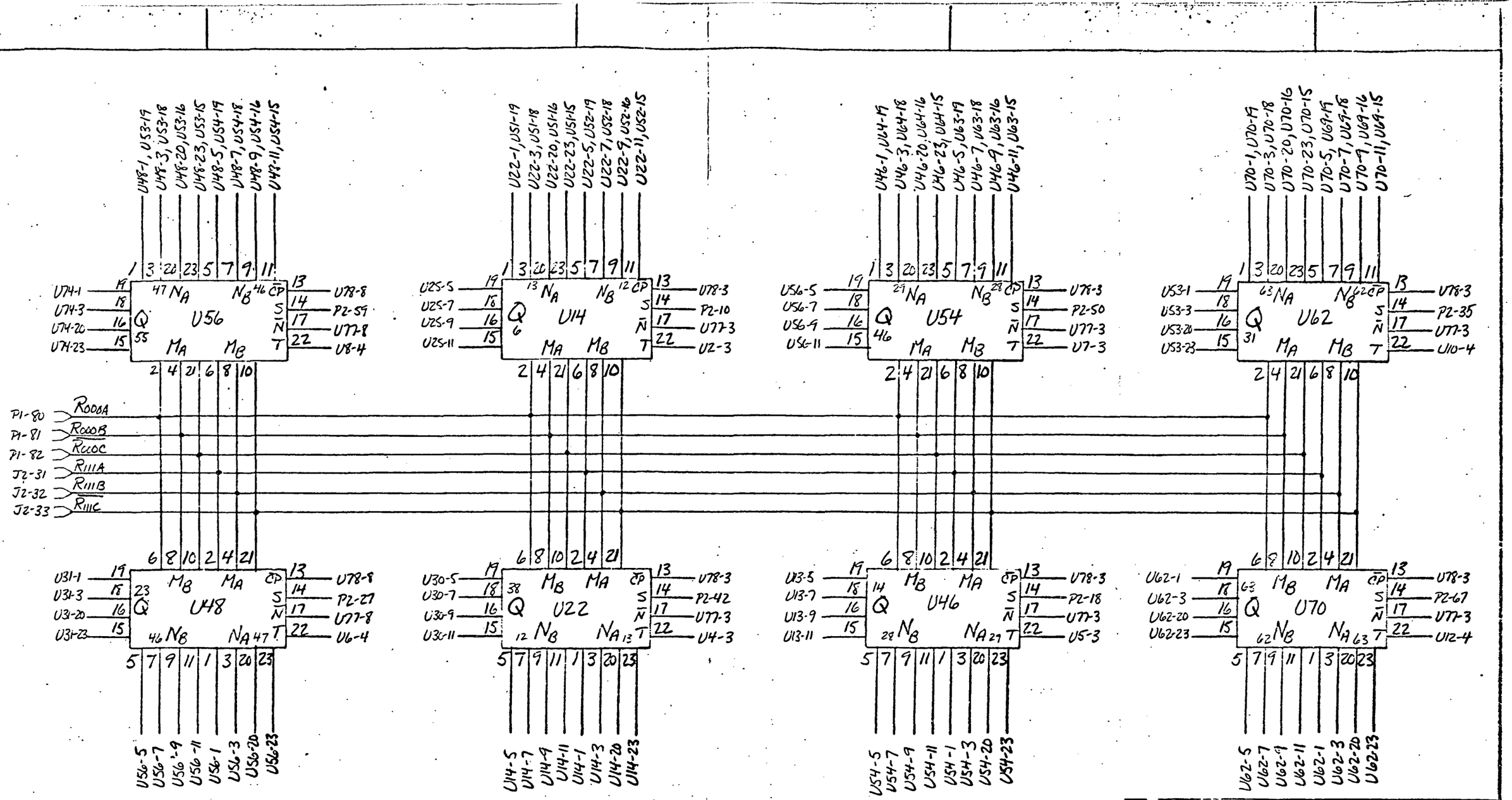
ARITHMETIC BOARD

ACS FOR STATES USING PATH METRIC R000

ALL IC's 1046

V_{CC} - PIN 24

GND - PIN 12



ARITHMETIC BOARD

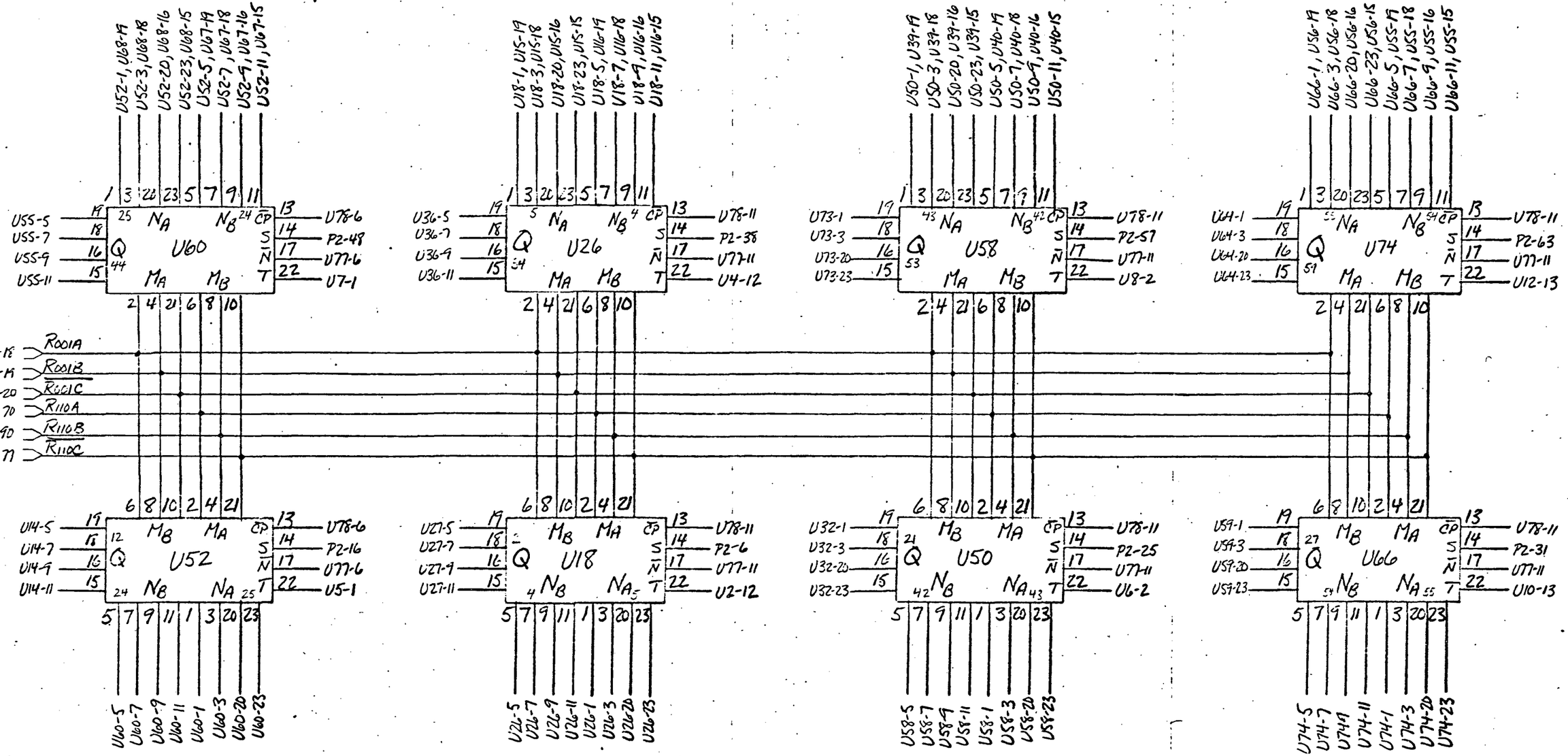
ACS FOR STATES USING PATH METRIC R000.

ALL IC'S 1046

V_{CC} – PIN 24

GND – PIN 12

FOLDOUT FRAME



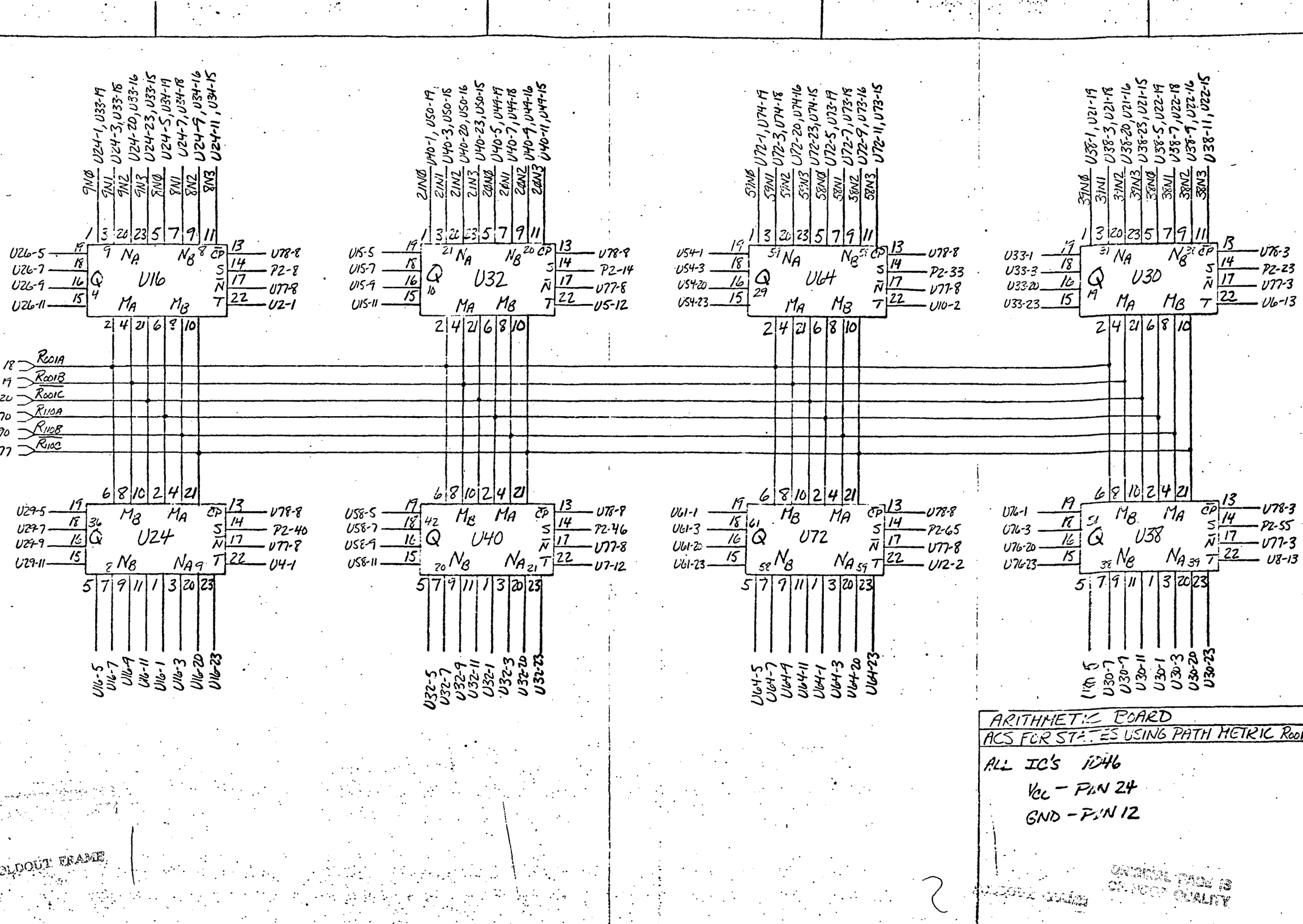
ARITHMETIC BOARD

ACS FOR STATES USING PATH METRIC R001.

ALL IC's 1046

V_{CC} - PIN 24

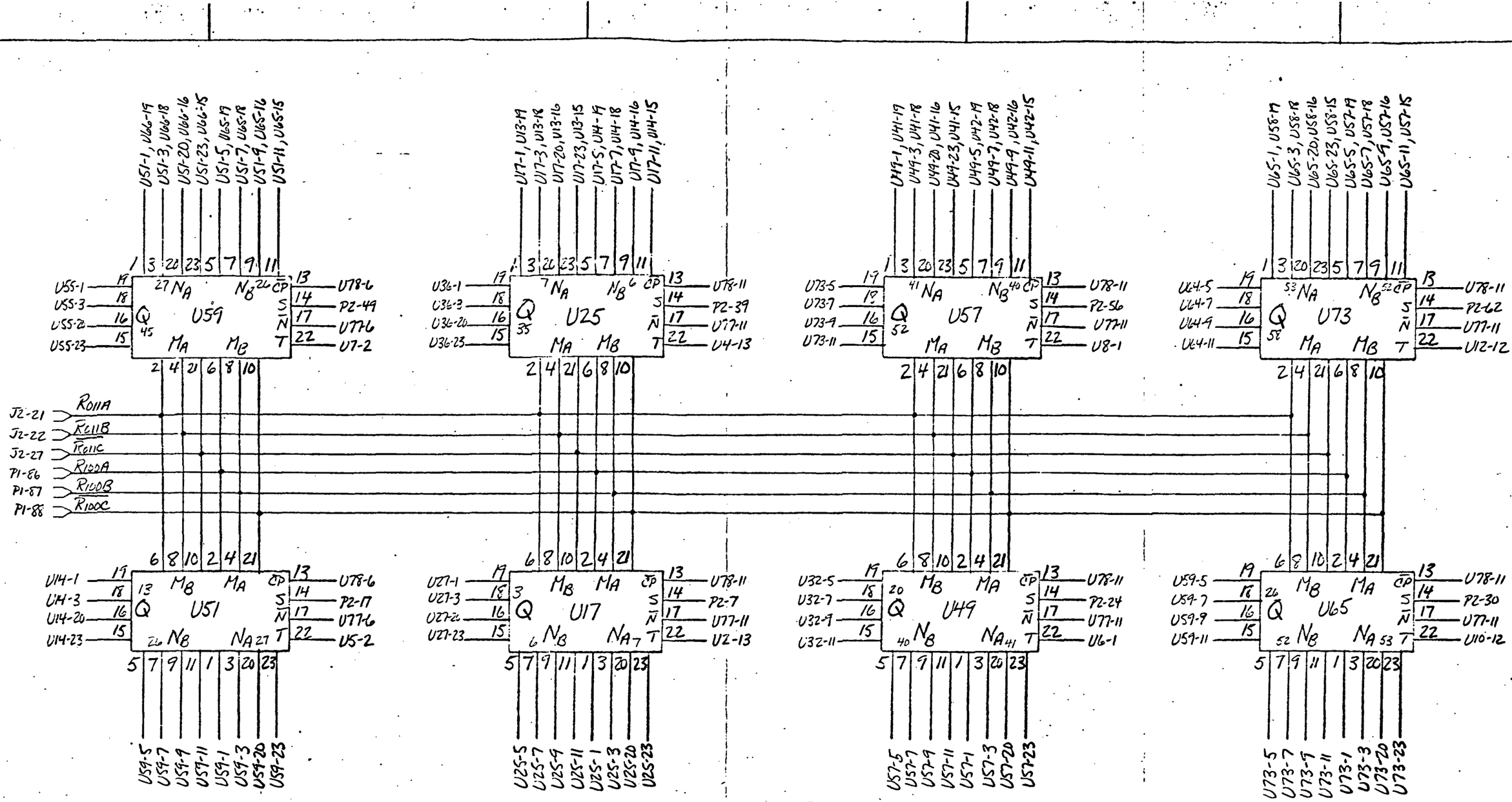
GND - PIN 12



ARITHMETIC BOARD
ACS FOR STATES USING PATH METRIC R001

ALL IC'S 10446
V_{CC} – PIN 24
GND – PIN 12

FOLDOUT FRAME



ARITHMETIC BOARD

ACS FOR STATES USING PATH METRIC R011

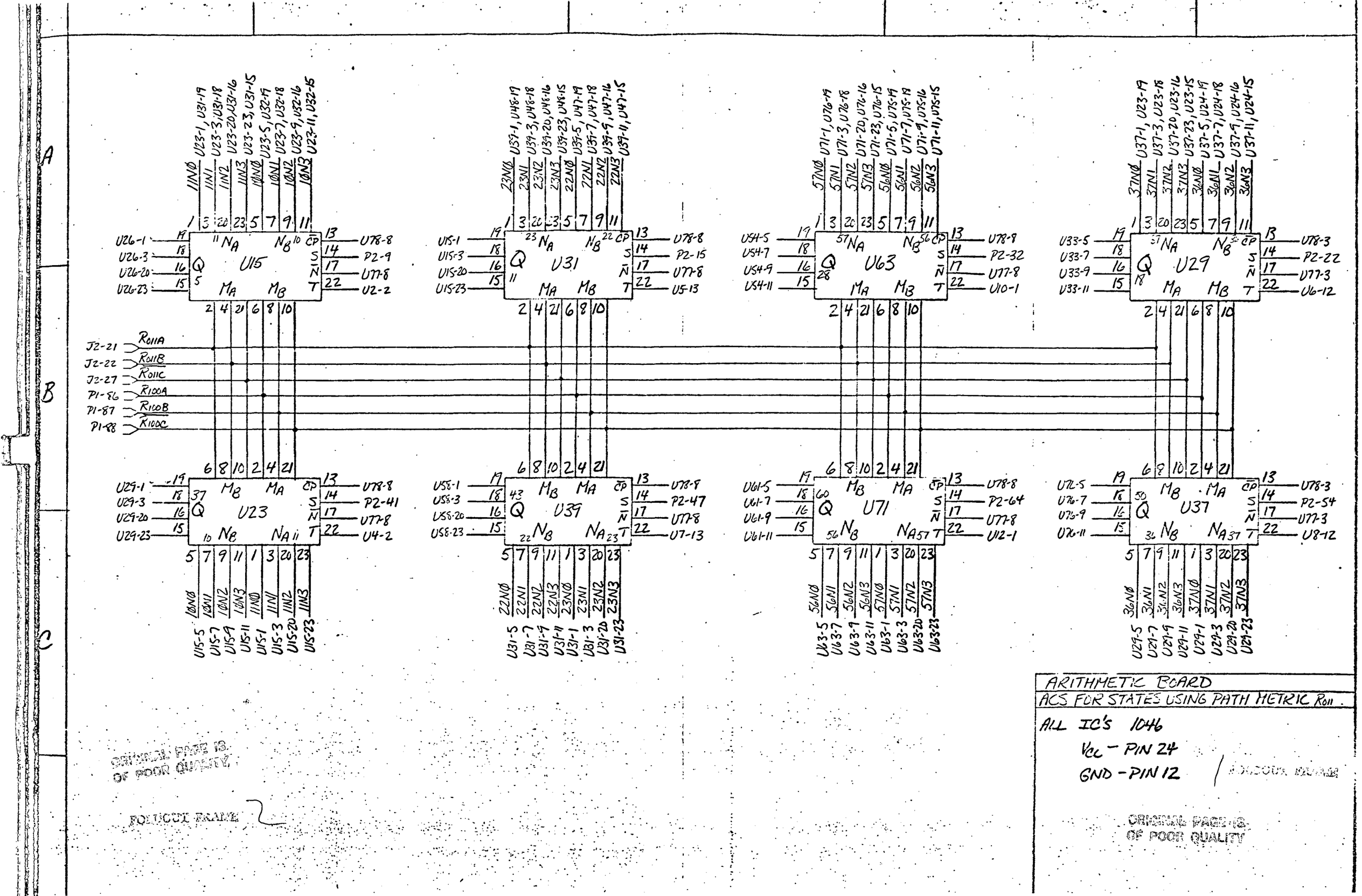
ALL IC'S 1046

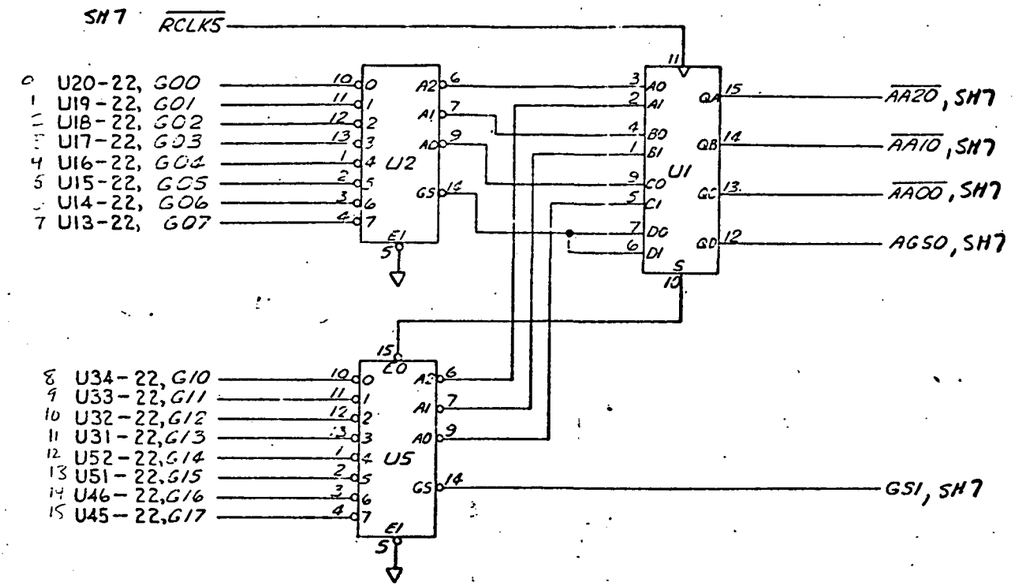
V_{CC} - PIN 24

GND - PIN 12

FOLDOUT FRAME 2

FOLDOUT FRAME


A
B
C
U115
U31
U63
U29
U23
U39
U71
U37
R011A
R011B
R011C
R100A
R100B
R100C
J2-21
J2-22
J2-27
P1-86
P1-87
P1-88
ARITHMETIC BOARD
ACS FOR STATES USING PATH METRIC R011
ALL IC's 1046
Vcc - PIN 24
GND - PIN 12
FOLDOUT FRAME
ORIGINAL PAGE IS OF POOR QUALITY



REF. DES	PART NO
U1	74298
U2	74148
U5	74148

1-

2- ORIGINAL PAGE IS OF POOR QUALITY

FOLDOUT FRAME

ORIGINAL PAGE IS OF POOR QUALITY

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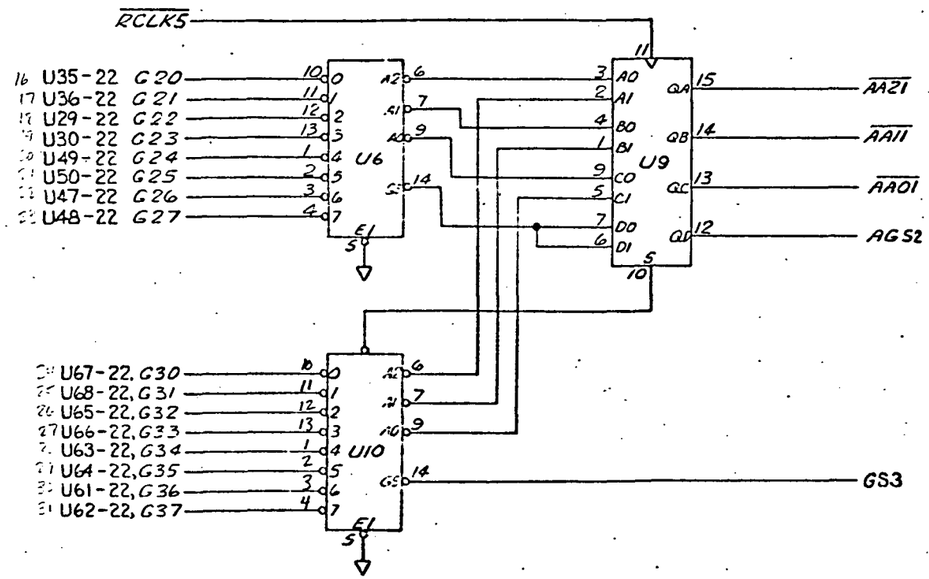
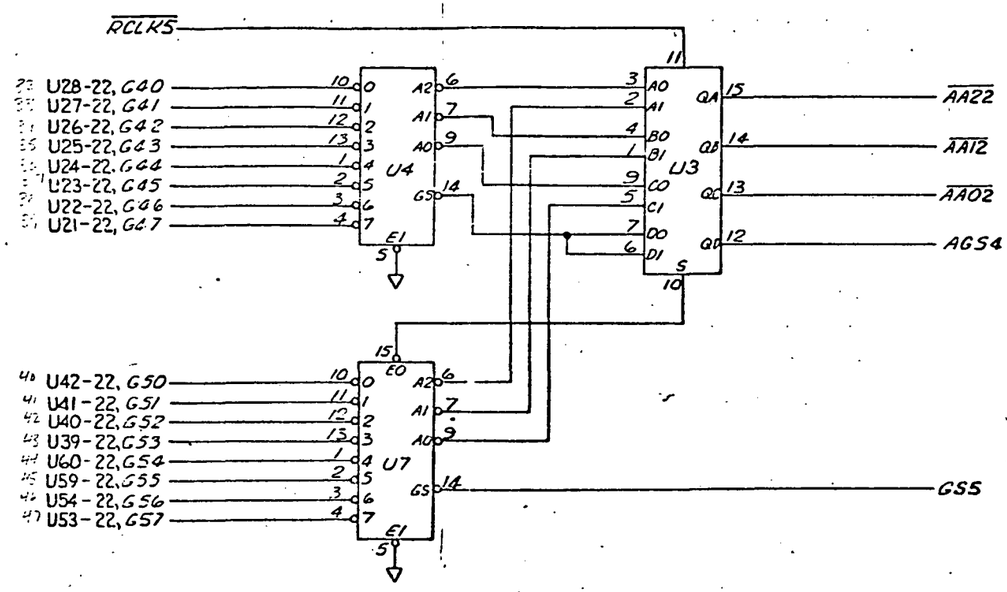
C	11627	40 21369
SCALE –	REVISION 5	SHEET 5



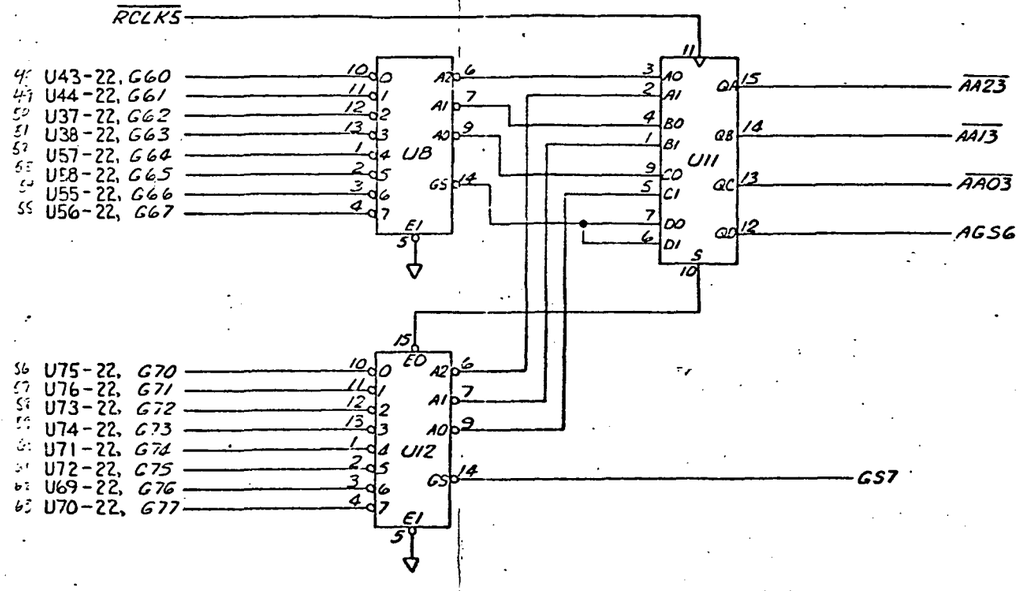
REF. DES.	PART NO.
U9	74298
U6	74148
U10	74148

SIZE	CODE IDENT NO	DRAWING NO	LD21369
C	11627	-	
SCALE -	REVISION B	SHEET 4	



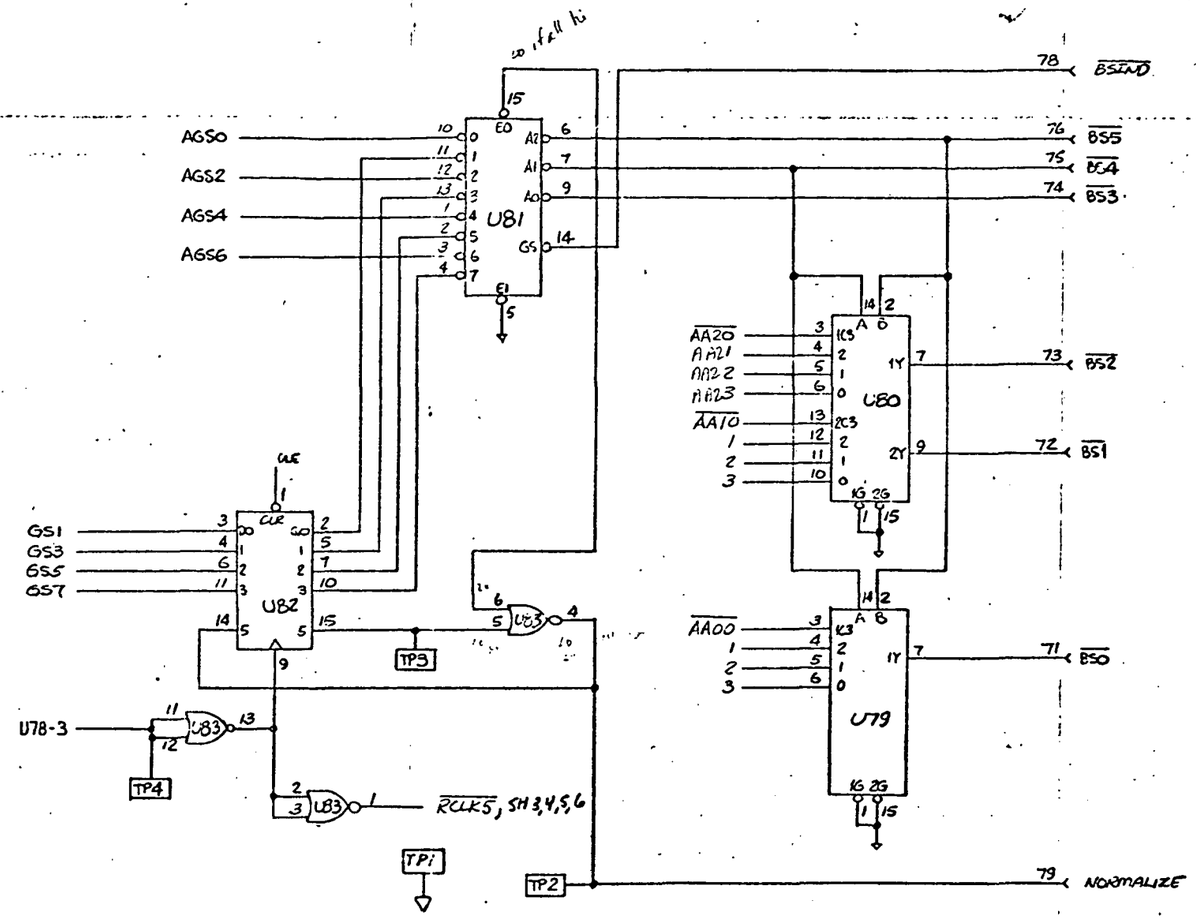
REF. DES.	PART NO
U4	74148
U3	74298
U7	74148

SIZE	CODE IDENT NO	DRAWING NO	LD21369
C	11627		
SCALE —	REVISION B	SHEET 5	



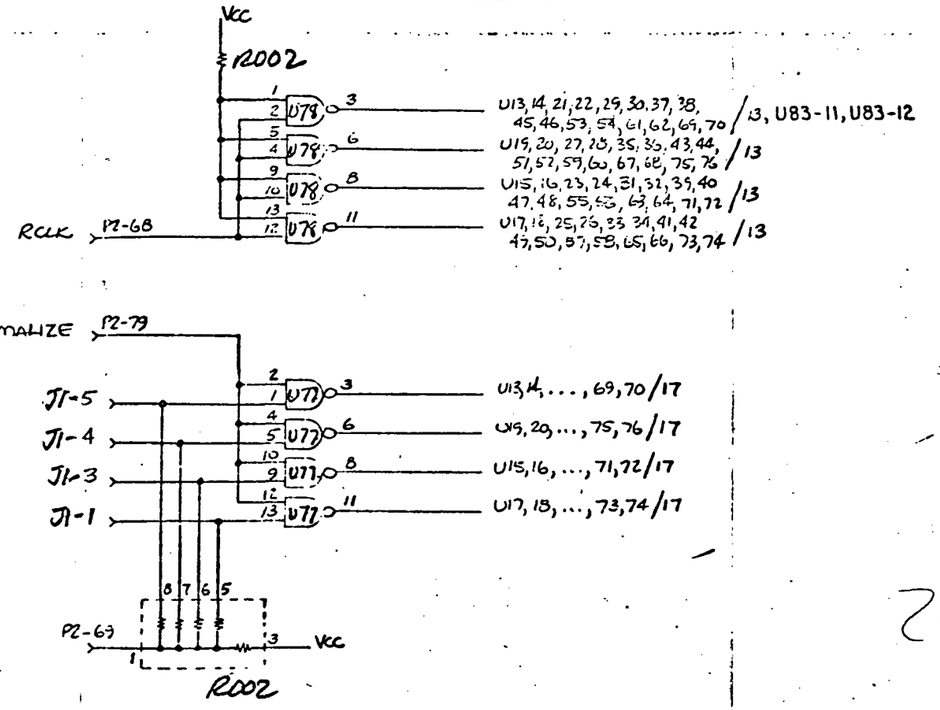
REF DES	PART NO
U8	74148
U11	74298
U12	74148

SIZE	CODE IDENT NO	DRAWING NO
C	11627	LD21369
SCALE --	REVISION B	SHEET 6



REF. DES	PART NO	
U79	74S153	– DUAL 4:1 MUX
U80	74S153	
U81	74148	PRIORITY ENC.
U82	74S174	
U83	74128	

SIZE	CODE IDENT NO	DRAWING NO	
C	11627		LD21369
SCALE –	REVISION		SHEET



REF DES	PART NO
U77	74S37
U78	74S37
R002	COMP. CARRIER

FOLDOUT FRAME

FOLDOUT FRAME

SIZE	CODE IDENT NO	DRAWING NO	LD21369
C	11627		
SCALE —	REVISION B	SHEET 8	

ARITH. PATH MEMORY J1. J10 INTL

+5V

WORD0 WORD1 WORD2 WORD3 WORD4 WORD5 WORD6 WORD7 WORD10 WORD11 WORD12 WORD13 WORD14 WORD15 WORD16 WORD17 WORD20 WORD21 WORD22 WORD23 WORD24 WORD25 WORD26 WORD27 WORD30 WORD31 WORD32 WORD33 WORD34 WORD35 WORD36 WORD37 WORD40 WORD41 WORD42 WORD43 WORD44 WORD45 WORD46 WORD47 WORD50 WORD51 WORD52 WORD53

SGNI+ SGNI- MSBI+ MSBI- LSBI+ LSBI- SGNQ+ SGNQ- MSBQ+ MSBQ- LSBQ+ LSBQ-

TDMA MODE CONTROL

RCLK

DRATE

FRAME+ FRAME-

J2

19 O/QPSK
18 ENCQ/PSK

20 DECQ/PSK
10 DRCLK+
DRCLK-
9 D2RCLK-
7 CHANERS-
23 D2RCLK+
6 DRCLK-
16
22 CHANERS+ D2RCLK+
15 DECDATA-
13
12 DECDATA+
4 ENCIDAT-
3 ENCIDAT+
10 ENCQDAT+
9 ENCQDAT-
1 E2RCLKO-

J3

19 MODEM SGNI+
18 MODEM SGNI-
16 MODEM MSBI+
15 MODEM MSBI-
13 MODEM LSBI+
12 MODEM LSBI-

10 MODEM, DINTL RCLK IN+
9 MODEM, DINTL RCLK IN-
7 MODEM, DINTL 2RCLK IN-
6 MODEM, DINTL 2RCLK IN+
4 MODEM, INTL. DATA OUT-
3 MODEM, INTL. DATA OUT+
1 MODEM, INTL 2RCLK OUT-
37 MODEM, INTL. 2RCLK OUT+

FOLDOUT FRAME

PATH ARITH J1 I/O INTL J3

WORD54 WORD55 WORD56 WORD57 WORD60 WORD61 WORD62 WORD63 WORD64 WORD65 WORD66 WORD67 WORD70 WORD71 WORD72 WORD73 WORD74 WORD75 WORD76 WORD77

J2

37 E2RCLKO+
35 E2RCLKO-
34 E2RCLKO+ EDATAIN+
7
4 E2RCLKI- EDATAIN-
6
3 E2RCLKI+
1 E2RCLKI-
37 E2RCLKI+
35 DSYNC+
34 DSYNC-

RIIA BS0 BS1 BS2 BS3 BS4 BS5 RIIC BSIND NORMALIZE RCCA ROOB ROOC RO1A RO1B RO1C RILA RIOB RIIC GND RIIB GND GND RCLOCK

DECODED OUTPUT

INTL RCLK OUT- 35
INTL RCLK OUT+ 34
INTL SYNCOUT+ 32
INTL SYNCOUT- 31

J1 17 14 11 8 5 2 36 33 30 27 24 21

J2 17 14 11 8 5 2 36 33 30 27 24

FOLDOUT FRAME

-5V

MODIFIED

LV7017B MANUAL

APPENDIX C

TM 21370
March 1981

OPERATION AND MAINTENANCE MANUAL

FOR

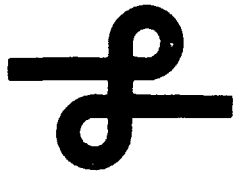
MODIFIED ENCODER-DECODER

AND

INTERLEAVER – DEINTERLEAVER

LV7017B

LINKABIT Part No. 21370



LINKABIT Corporation

TM 21370
March 1981

OPERATION AND MAINTENANCE MANUAL

FOR

MODIFIED ENCODER-DECODER

AND

INTERLEAVER – DEINTERLEAVER

LV7017B

LINKABIT Part No. 21370

LINKABIT Corporation
A M/A-COM Company
3033 Science Park Road
San Diego, CA 92121
714/453-7007
TWX 910-337-1277

WARRANTY

LINKABIT Corporation warrants the Modified Encoder-Decoder and Interleaver-Deinterleaver LV7017B to be free from defects in material, workmanship, and construction arising from normal usage. Its obligation under this Warranty is limited to replacing, or at its option, repairing any such defective equipment, which after regular installation and under normal usage and service, shall be returned within one (1) year from the date of original purchase to LINKABIT Corporation and which shall be found to have been thus defective in accordance with the policies established by LINKABIT Corporation.

LINKABIT Corporation assumes no liability for failure to perform or delay in performing its obligations with respect to this Warranty if such failure or delay results, directly or indirectly, from any cause beyond its control, including but not limited to, acts of God, acts of government, floods, fires, shortage of materials and labor and/or transportation difficulties.

This Warranty is expressly in lieu of all other agreements and warranties, express or implied, and LINKABIT Corporation does not authorize any person to assume for it the obligations contained in this Warranty and neither assumes nor authorizes any representative or other person to assume for it any other liability in connection with such equipment.

The Warranty shall not apply to any equipment which shall have been repaired or replaced by anyone else other than LINKABIT Corporation or which has been subject to alternation, misuse, negligence or accident, or to any equipment which shall have had the serial number or name altered, defaced or removed.

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SECTION 1

INTRODUCTION

1.1 SCOPE

This manual describes the modified Encoder-Decoder and Interleaver-Deinterleaver LV7017B, hereinafter referred to as the encoder-decoder (figure 1-1). It includes installation, operation, and maintenance instructions. The manual provides instructions for cleaning and periodic inspection of the equipment, troubleshooting, and replacing repair parts. Maintenance functions beyond the scope of this manual are to be performed by the Contractor, LINKABIT Corporation, a M/A-COM Company, 3033 Science Park Road, San Diego, California 92121.

Section 2 provides preparation for use and installation instructions. Section 3 provides operating instructions. Section 4 describes the theory of operation, and section 5 contains maintenance instructions. Section 6 contains logic diagrams.

1.2 PURPOSE AND FUNCTION

The purpose of the encoder-decoder is to provide coding and decoding functions to improve the reliability of transmission of digital data in satellite communications links. The encoder-decoder is designed for use with modems installed in satellite communication ground terminals.

The encoder is connected to the modulator, which reproduces two-bit phase-shift keyed signals for each information bit input to

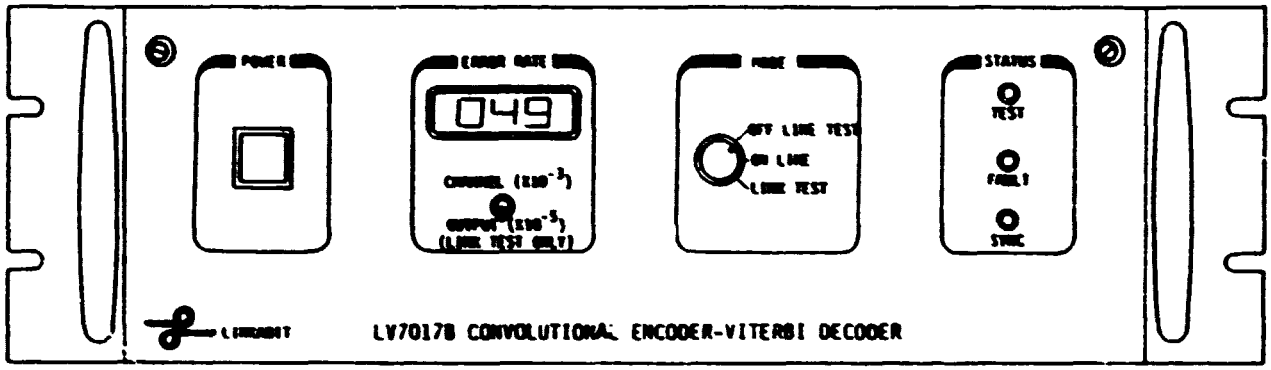

Figure 1-1. LV7017B Encoder-Decoder

the encoder. The decoder accepts the demodulator outputs and corrects errors without using a return communication link back to the encoder; thus it is described as a forward error correcting decoder. (A decoder which uses a return link for error correction is referred to as an automatic-repeat-request decoder.)

The encoding and decoding functions are independent and provide full duplex digital communication capability. The encoder-decoder will process data at any information rate from 0 bits-per-second (bps) up to 10 megabits-per-second (Mbps). The encoder-decoder has built-in test equipment for on-line and off-line self-tests. The encoder-decoder also generates a test signal which may be utilized by the communication channel for end-to-end testing.

1.3 DESCRIPTION

The encoder-decoder consists of a chassis assembly, two panel assemblies, and six circuit card assemblies (listed in table 1-1).

The encoder-decoder is of modular construction (figure 1-2) and mounts in a standard 19-inch equipment rack. The chassis assembly (with the front panel, rear panel, bottom and top covers) encloses six circuit card assemblies. The backplane circuit card assembly is mounted on the rear panel assembly and contains four receptacles for the plug-in circuit card assemblies. The display and control circuit card assembly is mounted on the front panel assembly. All controls and indicators

Table 1-1. Encoder-Decoder Assemblies

Item	Nomenclature	Reference Designator	Dwg. No.
1	Assembly, Chassis		21760
2	Panel Assembly, Front		21498
3	Panel Assembly, Rear		21494
4	Circuit Card Assembly, Arithmetic	A2	21369
5	Circuit Card Assembly, Input/Output	A5	21368
6	Circuit Card Assembly, Path Memory	A1	6042
7	Circuit Card Assembly, Display and Control	A3	21497
8	Circuit Card Assembly, Interleaver/Deinterleaver	A6	21373
9	Circuit Card Assembly, Backplane	A4	21493

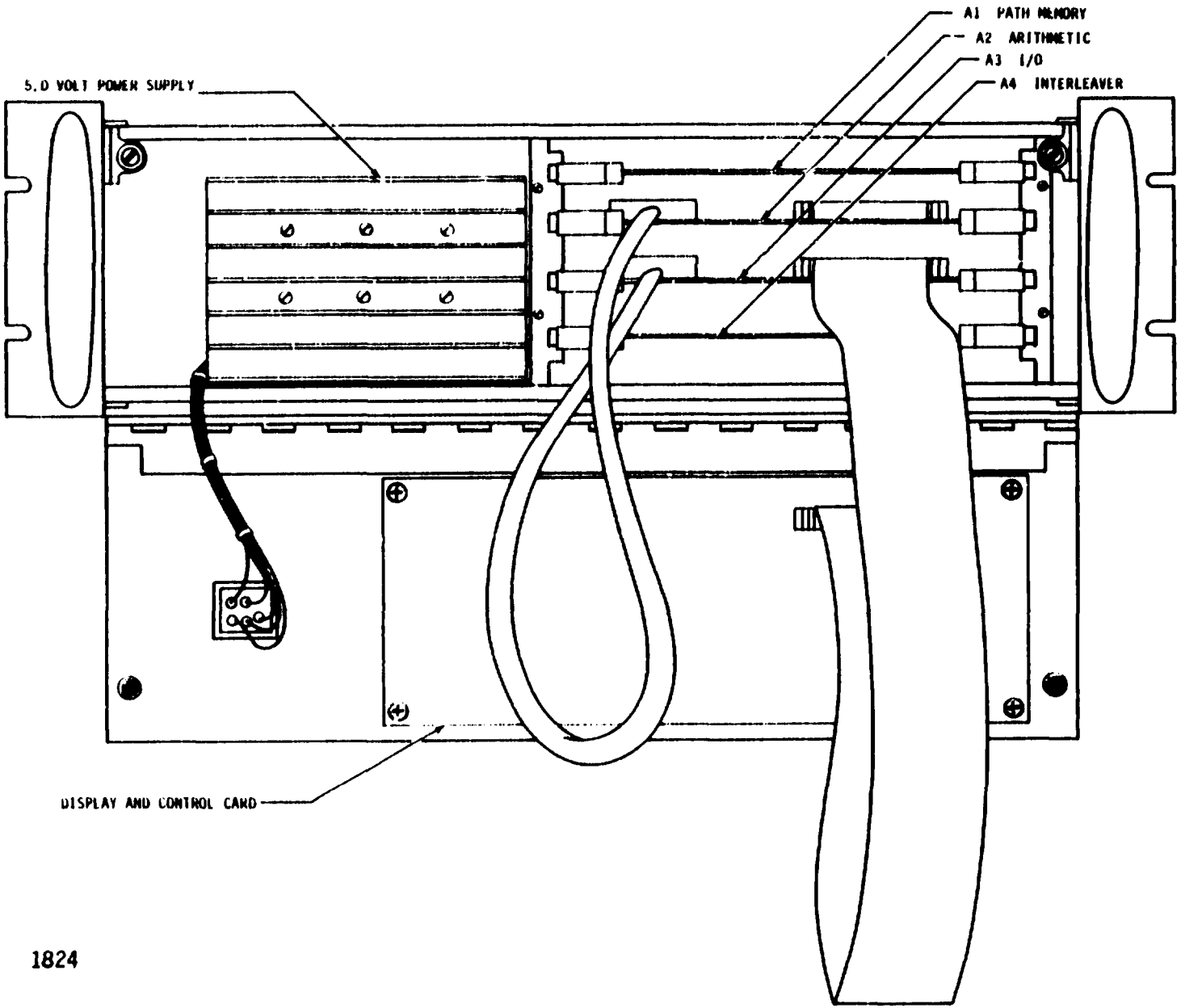

Figure 1-2. Encoder-Decoder Front View with Front Panel Lowered

for operation of the encoder-decoder are located on the front panel assembly (figure 1-1). The fan and all external connectors are located on the rear panel assembly (figure 1-3).

Plug-in circuit card assemblies A1, A2 and A5, A6 perform the encoding and decoding funtions.

The front panel assembly contains all controls and indicators for operating and testing the encoder-decoder. Controls and indicators are listed in table 3-1. The display and control circuit card assembly is attached to the back of the front panel assembly. The front panel assembly is hinged at the bottom to allow access to the display and control circuit card assembly and the plug-in circuit card assemblies. The plug-in circuit card assemblies are removed through the front.

The input/output (I/O) connectors J5, J6, J7 are mounted on the backplane circuit card assembly, which is part of the rear panel assembly (figure 1-3). I/O connector J6 contains all signals to and from the uncoded data source and sink. I/O connectors J5 and J7 have identical pinouts and contain all signals to and from the modem. J5 is used only when the interleaver/deinterleaver card is not installed. J7 is used only when this card is installed. The backplane circuit card assembly contains the four receptables (J1 through J4) for the plug-in circuit card assemblies. (The power connector is mounted on the rear panel assembly.)

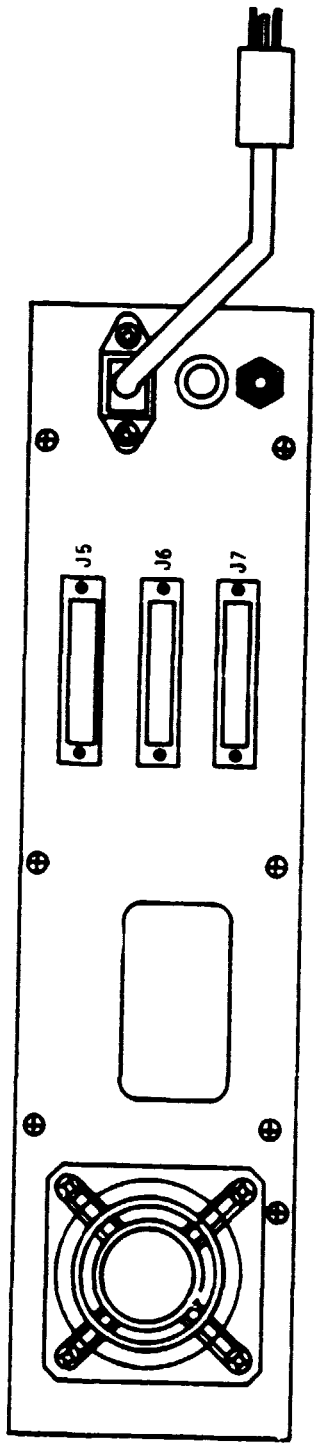

Figure 1-3. Encoder-Decoder Rear View

1.4 TECHNICAL CHARACTERISTICS

1.4.1 PRIME POWER REQUIREMENTS

Voltage	120 volts ac ±10%
Current	2.5 amps maximum
Frequency	60 Hz ±10%, single phase
Power	175 watts maximum

1.4.2 SERVICE CONDITIONS

Operation	Continuous
Temperature	+0°C to +50°C
Relative Humidity	30 to 70 percent
Elevation	Up to 10,000 feet

1.4.3 INTERFACE CHARACTERISTICS

Interface connections between the encoder-decoder and modem are accomplished via 75 ohm shielded, twisted-pair cables carrying balanced current mode signals. Driver and receiver circuit types and characteristics are as follows:

Line Driver	RS-422 AMD type AM26LS31
Line Receiver	RS-422 AMD type AM26LS32
Data Rate Capability	Any data rate from 0 to 6 Msymbols/sec
CLOCK Signals	Nominally one and zero for equal periods of time

1.5 SYSTEM APPLICATIONS

The encoder-decoder is capable of various modes of operation. Procedures for implementing these modes are contained in paragraphs 2.2.4.1 through 2.2.4.8. The various modes are all programmable by use of DIP switches or soldered jumper wires. The encoder is capable of operating in two different rates: rate 1/2 or rate 1/3.

The encoder-decoder is capable of operation with binary phase-shift keying (BPSK) modems, quadriphase-shift keying (QPSK) modems (rate 1/2 only), or offset quadriphase-shift keying (OQPSK) modems (rate 1/2 only). Refer to paragraphs 4.4 through 4.6.

A binary phase-shift keying modem modulates, transmits, receives, and demodulates one binary phase-shift-keyed waveform at a time. It does so by utilizing 0^{o} and 180^{o} phase-shift of a carrier.

A quadriphase-shift keying modem modulates, transmits, receives, and demodulates two parallel binary phase-shift-keyed waveforms simultaneously. It does so by utilizing 0^{o}, 90^{o}, 180^{o}, and 270^{o} phase shift of a carrier.

An offset quadriphase-shift keying modem modulates, transmits, receives, and demodulates two parallel binary phase-shift-keyed waveforms offset in time by one-half of the duration of the signal waveform.

The decoder will accept hard or soft decision data from the modem. (Refer to paragrah 4.1.) A hard decision is a one bit

output, 0 or 1, produced by the demodulator after processing one binary phase-shift-keyed waveform. A soft decision is a three bit output, 000, 001, 010, 011, 100, 101, 110, or 111, produced by the demodulator after processing one binary phase-shift-keyed waveform. One bit is identical to the hard decision output. The additional two bits available in soft decisions contain information about the quality of the demodulator output and therefore permit improved error correction performance by the decoder.

Off-line built-in test circuits are provided, enabling the encoder-decoder to monitor its own performance and to indicate to the operator when a malfunction occurs.

A loop-back test mode is provided in which the encoder output is connected to the decoder input through a built-in soft-decision channel simulator. The encoder clock and data inputs are internally generated and the decoder output can be monitored by means of the error rate counter. The loop-back mode is entered as the last step in the off-line built-in test sequence.

An internally generated data signal and output error detection circuits are provided so that end-to-end link tests can be performed. When the system is operating in its normal on-line mode, the encoder takes its data input from the internal pseudo-noise (PN) signal generator. The PN signal is encoded, modulated, and transmitted over the channel. The demodulated signal is decoded at the receiver. The decoded output can then be checked bit-by-bit for errors, since the data sequence is

known. The decoder output errors are fed to the error rate indicator, and the end-to-end link error rate can be monitored.

SECTION 2

PREPARATION FOR USE AND INSTALLATION INSTRUCTIONS

2.1 INSPECTION UPON RECEIPT

Equipment should be inspected upon receipt, as follows:

1. Inspect the equipment (unpacked) for damage incurred during shipment. If the equipment has been damaged, report the damage to the Contracting Officer.

2. Check the equipment (unpacked) against the packing list shipped with the equipment to see if the shipment is complete. Report all discrepancies to the Contracting Officer. The equipment should be placed in service even though a minor assembly or part that does not affect proper functioning is missing or damaged.

2.2 INSTALLATION INSTRUCTIONS

The encoder-decoder can be used in various applications described in paragraph 1.5. The operating options can be programmed by setting DIP switches or by connecting or disconnecting soldered jumper wires. The encoder-decoder is programmed for its intended operating configuration prior to deployment. If the desired operating mode is different from that which is installed in the encoder-decoder upon receipt of equipment, the encoder-decoder must be reprogrammed. Paragraphs 2.2.4 through 2.2.4.8 describe the methods for implementing the programmable installation options. These procedures can be performed before or after installation of the equipment in the rack.

2.2.1 SITE REQUIREMENTS

There are no specific site requirements for the encoder-decoder. The location of the encoder-decoder is determined by the terminal site.

2.2.2 TOOLS AND MATERIALS REQUIRED

The following tools and materials are required for installing the encoder-decoder:

1. Common hand tools
2. Soldering equipment (if installing a jumper for implementing a programmable option)
3. Hookup wire (size #22 AWG), if needed for connection of a programmable option.

2.2.3 ELECTRICAL CONNECTIONS

2.2.3.1 EXTERNAL POWER CONNECTION - After the encoder-decoder is installed in the equipment rack, connect the ac power cord assembly to the ac power source.

2.2.3.2 SIGNAL CONNECTIONS FOR NORMAL OPERATION - Encoder-decoder input/output signals and corresponding input/output pin connections are listed in tables 2-1 and 2-2. Connector J6 is the data source/sink connector and is always used. Connectors J5 and J7 are the modem connectors. Connector J5 is used only when there is no interleaver card in the encoder-decoder. Connector J7 is used only when the interleaver card is in the encoder-decoder.

Table 2-1. Data Source/Sink Connector Signal List

Pin Number (J6)	Signal	Description
1	-	Symbol rate clock to encoder
37	+ E2RCLKI	
36	Shield	
2	Shield	R Clock to encoder
3	+ ERCLKI	
4	-	
5	Shield	Data to encoder
6	- EDATAIN	
7	+	
8	Shield	Encoder Q-channel symbols to modem (QPSK only)
9	- ENCQDAT	
10	+	
11	Shield	Decoded data from decoder
12	+ DECDATA	
13	-	
14	Shield	R Clock from decoder
15	+ DRCLKO	
16	-	
17	Shield	
18	+ ENC B/$\bar{Q}$ PSK	Encoder BPSK/QPSK mode control
19	+ Q/$\bar{Q}$ PSK	Decoder Offset/QPSK mode control
34	-	Decoder sync status
35	+ DSYNC	
36	Shield	

Table 2-2. Modem Connector

Pin Number (J5 or J7)	Signal	Description
37	+	
1	-	ENC 2RCLKOUT — Symbol clock from encoder
2	Shield	
3	+	
4	-	ENC I DATA — In QPSK, I channel data from encoder. In BPSK encoded data from encoder
5	Shield	
6	+	
7	-	D2RCLK — Symbol clock to decoder
8	Shield	
9	-	
10	+	D RCLK — R Clock to decoder
11	Shield	
12	-	
13	+	LSBI — LSB of 3 bit quantized symbol input to decoder (I Channel in QPSK)
14	Shield	
15	-	
16	+	MSBI — MSB of 3 bit quantized symbol input to decoder (I channel in QPSK)
17	Shield	
18	-	
19	+	SGNI — Sign bit of 3 bit quantized symbol input to decoder (I channel in QPSK)
33	Shield	
21	Shield	
22	+	CHANERS — Channel Error output
23	-	

Table 2-2. Modem Connector (Continued)

Pin Number	Signal	Description
24 (J5 only)	Shield	LSB of Q channel 3 bit quantized symbol input to decoder (QPSK only)
25 (J5 only)	- LSBQ	
26 (J5 only)	+	
27 (J5 only)	Shield	MSB of Q channel 3 bit quantized symbol input to decoder (QPSK only)
28 (J5 only)	- MSBQ	
29 (J5 only)	+	
30 (J5 only)	Shield	Sign bit of Q channel 3 bit quantized symbol input to decoder (QPSK only)
31 (J5 only)	- SGNQ	
32 (J5 only)	+	
30 (J7 only)	Shield INTL	Interleaver sync status
31 (J7 only)	+ SYNC	
32 (J7 only)	- OUT	
34 (J7 only)	+	R Clock from encoder
35	- ERCLKO	
36	Shield	
20	+ DEC B/$\overline{Q}$PSK	Decoder BPSK/QPSK mode control

2.2.4 IMPLEMENTATION OF INSTALLATION OPTIONS

The following paragraphs describe the methods of implementing the internal programmable installation options if the desired operating mode is different from that which is installed upon receipt of the equipment. The terminals to be soldered and the switches to be set are located on the I/O card, with the exception of the interleaver bypass switch which is located on the Interleaver Card. Refer to figure 1-2 for the locations of these cards.

In normal on-line operation, the two ends of the link each require their own encoder-decoder; the encoder portion is associated with the transmit end, and the decoder with the receive end. Both of these encoder-decoders must be programmed for the same mode of operation.

2.2.4.1 BPSK, QPSK OR OQPSK INTERFACE - The encoder-decoder is factory programmed to operate in BPSK mode. To select QPSK mode, ground J6-18 and J5-20 on the back panel connectors. To select OQPSK mode, ground J6-18, J6-19 and J5-20.

2.2.4.2 HARD OR SOFT DECISION MODE - The encoder-decoder is factory programmed to operate in soft decision mode. To select hard decision mode, install a #22 AWG wire jumper between P1-27 and P1-89 on the I/O Card.

2.2.4.3 REVERSE GENERATORS - The encoder-decoder is factory programmed so that the code generator DIP switches are set to NORMAL. To reverse encoder code generators, turn DIP switch 1 to

OFF. (Switch is off when side marked ON is up.) To reverse decoder code generators, turn DIP switch 8 to ON in BPSK and to OFF in QPSK. For rate 1/3 operation, these switches must be set to NORMAL; i.e., switch 1 to ON, switch 8 to OFF.

2.2.4.4 DIFFERENTIAL CODING - To select differential encoding, turn DIP switch 2 to OFF. To select differential decoding, turn DIP switch 5 to OFF. The encoder-decoder is factory programmed to disable differential coding and decoding.

2.2.4.5 INVERTING ALTERNATE CHANNEL SYMBOLS - The encoder-decoder is factory programmed in the normal mode; i.e., alternate channel symbols are not inverted. The encoder will invert alternate channel symbols when DIP switch 3 is turned to OFF. The decoder will decode data with alternate channel symbols inverted when DIP switch 4 is in the ON position on the I/O Card.

2.2.4.6 CODE RATE - The encoder-decoder is factory programmed to rate 1/2 coding. To select rate 1/3 coding, turn DIP switch 6 on the I/O Card to the OFF position.

2.2.4.7 PATH MEMORY - LINKABIT makes two different path memory cards with different delays. The path memory switch assures compatibility with each delay. Normal operation is with the I/O Card DIP switch 7 turned to ON. The encoder-decoder is factory programmed in the normal mode.

NOTE

The path memory switch is not normally moved in the field.

2.2.4.8 INTERLEAVING - The encoder-decoder is factory programmed to disable symbol interleaving. Symbol interleaving may be selected by throwing the interleaver IN/OUT switch on the edge of the interleaver card to IN. When the interleaver card is installed, the data input to the encoder-decoder from the modem must use connector J7. The encoder-decoder will operate with the interleaver card removed if the modem connector J5 is used. The interleaver card may only be used in the BPSK mode of operation.

SECTION 3
OPERATING INSTRUCTIONS

The encoder-decoder may be used in three modes: duplex link communication, link test, and self test. Duplex link communication is the normal mode of operation for the encoder-decoder. In this mode, the encoder-decoder provides channel error correction for the communication link. The link test mode is used to determine channel quality from modem to modem. Full duplex channel testing can be performed using link test procedures.

Self test procedures are performed for fault isolation and to ensure that the encoder-decoder is operating properly. On-line tests provide continuous monitoring, both dynamic and static, of various circuit parameters when the encoder-decoder is in the on-line (normal) duplex link mode of operation (paragraph 3.4). A detailed description of the self-test functions is provided in paragraphs 4.9, 4.10, and 4.11.

3.1 CONTROLS AND INDICATORS

Encoder-decoder controls and indicators are shown in figure 1-1 and described in table 3-1.

Table 3-1. Controls and Indicators

Control/Indicator	Position	Function
MODE, Rotary Switch	OFF-LINE TEST	Places encoder-decoder in the internal self-test mode.
	ON-LINE TEST	Normal mode for operation in the communication link.
	LINK TEST	Selects an internally generated 2047 bit pseudo noise sequence for data to be encoded and transmitted over the communication link.
ERROR RATE 2-position toggle switch	CHANNEL($x10^{-3}$)	Causes ERROR RATE display to display channel symbol error rate.
	OUTPUT($x10^{-5}$) (LINK TEST ONLY)	In LINK or OFF-LINE test mode, causes ERROR RATE display to display decoder output bit error rate. In ON-LINE mode display always displays channel error rate.
STATUS TEST momentary push button	Depressed	When the MODE Switch is in OFF-LINE TEST, initiates the encoder-decoder self test.
FAULT Indicator		Illuminates when a fault exists in the encoder-decoder.

Table 3-1. Controls and Indicators (Continued)

Control/Indicator	Position	Function
SYNC Indicator		Illuminates when the decoder is in sync.
ERROR RATE display		Displays channel error rate as a multiple of 10^{-3} or output error rate as a multiple of 10^{-5} as determined by switch setting.
POWER Switch		Applies prime power to the encoder-decoder.

3.2 INITIAL CONTROL SETTINGS

Before placing the encoder-decoder into operation, the site requirements must be reviewed, and the following control settings should be made:

CAUTION

Ensure that the POWER switch is in the OFF position when prime site power is applied, to avoid damage to internal circuits of the encoder-decoder.

1. Set POWER switch to OFF before applying prime site power.

2. After prime site power is applied, set controls for normal operation, as described in table 3-2.

3.3 NORMAL OPERATION

For normal operation (on-line) the encoder-decoder is placed in the duplex link communication mode of operation, as follows:

1. Ensure controls are set as shown in table 3-2.

2. Place MODE switches of encoder-decoders at both ends of the link in the ON-LINE position. The normal duplex link is now established.

3. At the receive terminal, measure the channel error rate by using the ERROR RATE counter, as described in paragraph 3.6.

Table 3-2. Control Settings for Normal Operation

Control	Setting	Indicator	Required Indication
MODE	ON LINE		
POWER	ON	POWER	Illuminated
ERROR RATE	CHANNEL ($x10^{-3}$)	SYNC	Illuminated
		FAULT	Extinguished
		ERROR RATE Counter	Detected channel error rate

3.4 OFF-LINE TESTS

Off-line tests are controlled by a microprogrammed processor and consist of fault isolation and loop-back tests. The fault isolation circuitry detects a go or no-go condition. When the fault isolation sequence is terminated, the processor is programmed to initiate a loop-back test which provides a simulated channel condition signal to the encoder. During the loop-back test the simulated channel error rate of the decoder output rate may be selected and displayed on the ERROR RATE counter (paragraph 3.6). The off-line test program also contains provisions for inserting a fault into the encoder-decoder and indicating whether or not the fault isolation tests detect the fault.

CAUTION

Performing off-line tests on the encoder-decoder will interrupt digital user communication on either link, transmit, or receive, if the modem is programmed for external error coding of the LV7017 encoder-decoder.

1. Put the MODE switch in OFF-LINE TEST position.

2. To perform a loop-back test, momentarily depress the TEST pushbutton. Initially, the FAULT indicator will illuminate momentarily, after which the GO indicator will illuminate and remain illuminated. (Refer to paragraph 4.11 for explanation of the sequence.) Also, the STATUS SYNC indicator is illuminated.

3. Repeat step 2 several times. When the GO indicator remains illuminated, the encoder-decoder is performing properly.

NOTE

Depressing the TEST pushbutton automatically initiates the loop-back test (see step 2). This action will commence approximately 3 seconds after operating the TEST pushbutton, and will remain in this mode until the unit is taken out of the test mode (MODE switch is ON LINE or LINK TEST) or until self-test is reinitiated by depressing the TEST pushbutton.

4. During the test in step 2, use the procedures in paragraph 3.6 to measure simulated channel error rate or decoded output error rate. The ERROR RATE counter should indicate 050 ±10% for the channel error rate and less than 006 for the output error rate. (See paragraph 4.11.)

3.5 END-TO-END LINK TEST

Full duplex channel testing can be performed during the end-to-end link test. To perform an end-to-end link test, proceed as follows:

1. If the encoder-decoder is nonoperational, set the switches as shown in table 3-2, except select LINK TEST.

2. Place MODE switches of the encoder-decoders at both ends of the link in the LINK TEST position for LINK TEST operation. The end-to-end link test has now been initiated.

3. Measure either channel error rate or decoder output error rate (paragraph 3.6) at the receive terminals by using the ERROR RATE counter. The decoder error rate measurement gives a measure of performance of the entire communication system from the encoder input at the transmit end to the decoder output at the receive end of the link.

3.6 USE OF THE ERROR RATE COUNTER

The ERROR RATE counter can be used to measure either channel error rate or decoder output error rate. However, the decoder output error rate can be measured only when the encoder-decoder is in the OFF-LINE TEST or LINK TEST modes.

To use the ERROR RATE counter, proceed as follows:

1. Change the error source from channel errors to output errors, or from output errors to channel errors, by changing the setting of the CHANNEL/OUTPUT switch.

2. When measuring CHANNEL error rate, multiply the 3-digit output shown on the ERROR RATE display by 10^{-3} (0.001). Thus 013 becomes 013 x 0.001 = .013.

3. When measuring OUTPUT error rate, multiply the 3-digit output by 10^{-5} (0.00001). Thus 056 x 0.00001 = .00056.

NOTE

The maximum count is 999 on the 3-digit indicator. This can never be exceeded when measuring channel error rate. If the maximum count is exceeded when measuring output error rate, this can be taken to be an indication of a malfunction somewhere in the system.

SECTION 4
THEORY OF OPERATION

4.1 INTRODUCTION

The encoder-decoder enhances communication system performance over a satellite link by correcting errors due to noisy environment. The error correction process begins by adding redundancy to a digital data stream by means of an encoder located at the transmit end of the link. At the receive end, a decoder uses this redundancy to correct almost all the errors introduced by the channel.

Encoding is accomplished by means of a convolutional encoder having a code rate of 1/2 or 1/3 and a constraint length of seven. The rate 1/2 refers to the fact that each information bit into the encoder is encoded into two channel symbols. Similarly, the rate 1/3 refers to the fact that each information bit into the encoder is encoded into three channel symbols. A constraint length of seven indicates that the encoder outputs, when an information bit is input, are determined by the present information bit and the previous six information bits.

The decoder is implemented using a technique known as the Viterbi decoding algorithm. The symbols received from the channel, and thus potentially noisy, are fed to the decoder by the demodulator. The decoder outputs one information bit for each two or three symbols, depending on code rate. Due to the complexity of the Viterbi algorithm, there is a delay of 72 bit times from the time the channel symbols enter the decoder to the

time the associated information bit emerges in its decoded form at the decoder output.

The decoder can accept demodulated data in either of two formats (paragraph 1.5). The first, termed hard decision, involves each demodulated symbol being represented as a logical "1" or a logical "0". This is the most common form for digital data. In the second format, termed soft decision, each symbol is represented by three bits: a sign bit, which is identical to the hard decision output, plus two magnitude bits which give a measure of the quality of the data. Use of soft decision data yields a significant performance improvement over hard decision (paragraph 4.2).

A technique known as differential coding is often used to eliminate certain ambiguities present in BPSK and QPSK modems. The technique involves reformatting the original data stream into one in which information is contained in symbol transitions. The encoding process looks at the present information bit and the previous transmitted symbol. If the present information bit is a one, the differentially encoded symbol is the inverse of the previous transmitted symbol. If the present information bit is a zero, the differentially encoded bit is the same as the previous transmitted symbol. To differentially decode, a one is output whenever the received symbol changes and a zero when there is no change.

With the interleaver card installed and switched in, coded symbols are interleaved by a periodic interleaver. After

demodulation, received channel symbols are then deinterleaved. This process is used to diminish the effects of bursts of noise by spreading the burst over widely scattered (in time) symbols.

4.3 CODING GAIN

The transmission of digital data over a satellite communications link typically results in random errors in the data sent from the demodulator to the data sink. These errors are primarily caused by the noise inherent in the satellite link. The performance of a digital communication link is generally measured in terms of the average bit error rate at the digital output of the link. Average bit error rate is determined by dividing the number of bit errors occurring in a large sample of bits by the total number of bits in the sample. The resulting number is the bit error probability, also referred to as the average bit error rate. For example, if it is determined that 40 errors have occurred in a total of 10,000 bits, the bit error probability is 40/10,000 or 4×10^{-3}.

The bit error probability produced by a satellite communications link is a function of the data rate and the signal-to-noise ratio present at the modem receiver input. At higher data rates, more signal power is required to achieve the same error rate. Ideally, the dependence of bit error probability on data rate for a given signal-to-noise ratio may be removed by redefining signal-to-noise as

F_b/N_o = signal power to noise power in bandwidth equal to data rate.

Alternately, this ratio can be viewed as the ratio of the signal energy in one bit (E_b) to noise power in one cycle of bandwidth (N_o) alternately termed noise density. The bit error probability as a function of E_b/N_o can now be plotted as a single curve for all data rates as illustrated in figure 4-1.

As shown in figure 4-1, if only differential coding is used, the signal-to-noise ratio (E_b/N_o) required to obtain a low bit error rate is higher than that required to obtain the same error rate with either hard or soft decision rate 1/2 decoding. For example, if a user required an error rate equal to or less than 1×10^{-5}, the minimum signal-to-noise ratio (E_b/N_o) needed to support this requirement using only differential coding is +9.5 dB. If Viterbi soft decision rate 1/2 decoding is used, the signal-to-noise ratio required is reduced to +4.5 dB. Stated another way, it can be said that rate 1/2 Viterbi soft decision decoding provides a coding gain of greater than 5 dB. Using this definition, it is seen that the coding gain for hard decision operation is about 3 dB, illustrating the 2 dB performance improvement afforded by soft decision over hard decision operation.

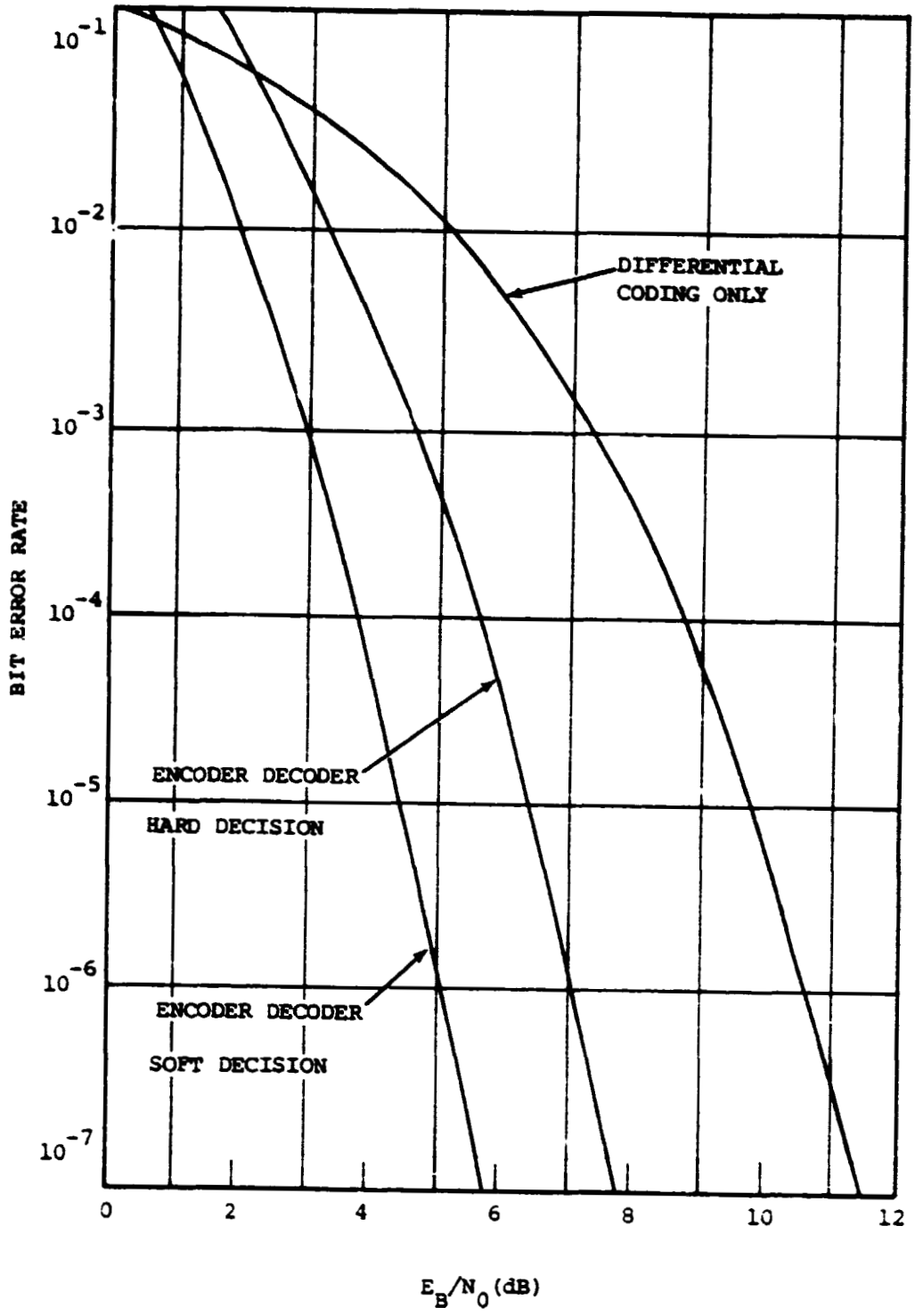

Figure 4-1. Theoretical PSK Modem Bit Error Rate Performance for Various Rate 1/2 Coding Configurations

4.3 INTERFACE AND TIMING

Since the encoder-decoder will operate with both PSK and QPSK modems, the encoder-decoder must be capable of accepting/ generating either one serial rate S symbol stream or two parallel rate R symbol streams. The clock signals are of such frequency that one cycle of the R clock is equal to a unit interval of the data signal and two (or three in rate 1/3) cycles of the S clock are equal to one unit interval of the data signal. The relationships of the receiver and transmitter data and clock interfaces for BPSK and QPSK are shown in figures 4-2, 4-3, and 4-4. The OQPSK data format is shown in figure 4-5. The functional interfaces for serial (BPSK) and parallel (QPSK and OQPSK) operation are described in paragraphs 4.4, 4.5, and 4.6.

4.4 SERIAL SYMBOL STREAM (BPSK MODEM)

In the serial symbol mode, the encoder-decoder interfaces with a BPSK modem (figure 4-6). The modulator accepts the data at rate R, conditions it, and interfaces with the convolutional encoder. The encoder returns a single coded stream of encoded symbols at rate S to the modem. At the receive end of the link, the modem output (either hard or soft decision), is interfaced with the decoder at rate S for Viterbi decoding. The decoded data is returned to the demodulator for output conditioning. The appropriate clock accompanies data across all interfaces.

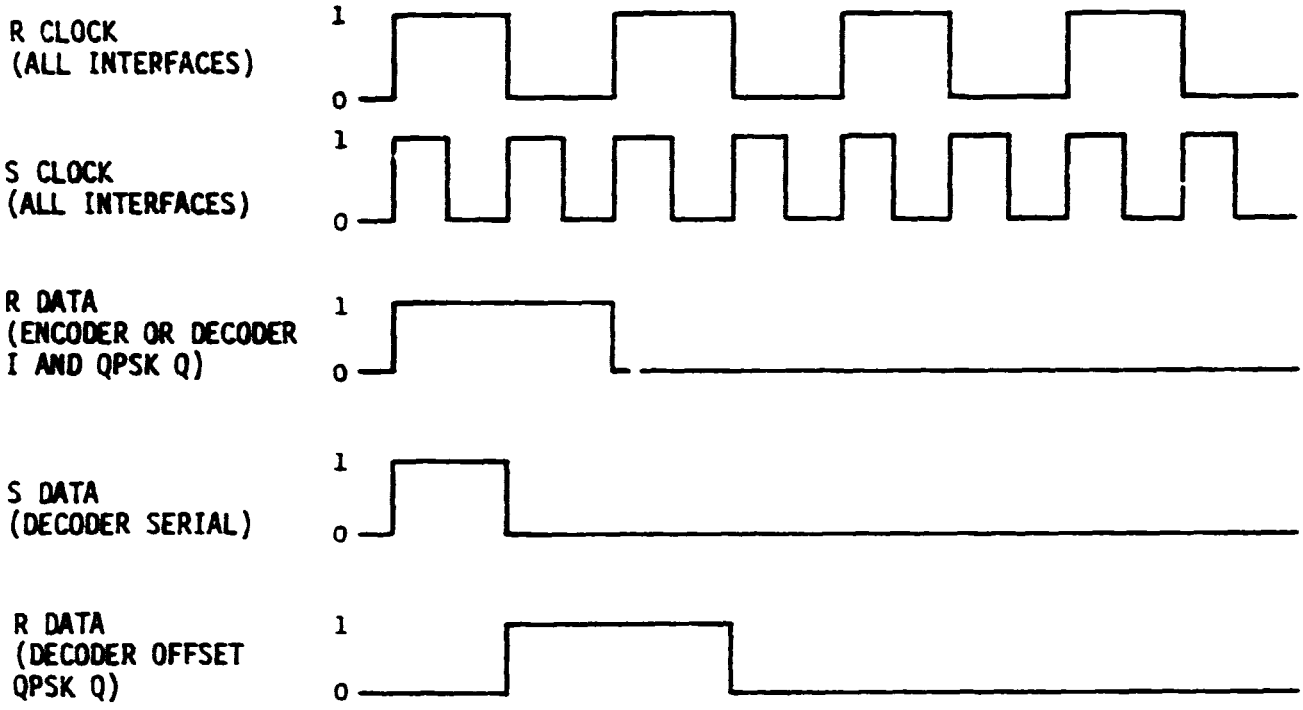

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Figure 4-2. Receiver Data and Clock Relationships, Rate 1/2

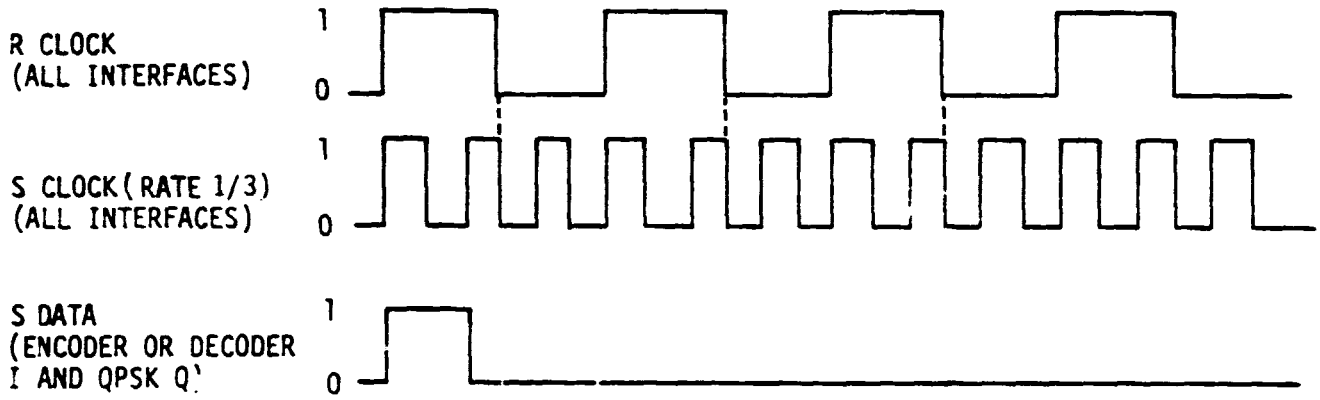

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Figure 4-3. Transmitter and Receiver Data and Clock Relationships, Rate 1/3

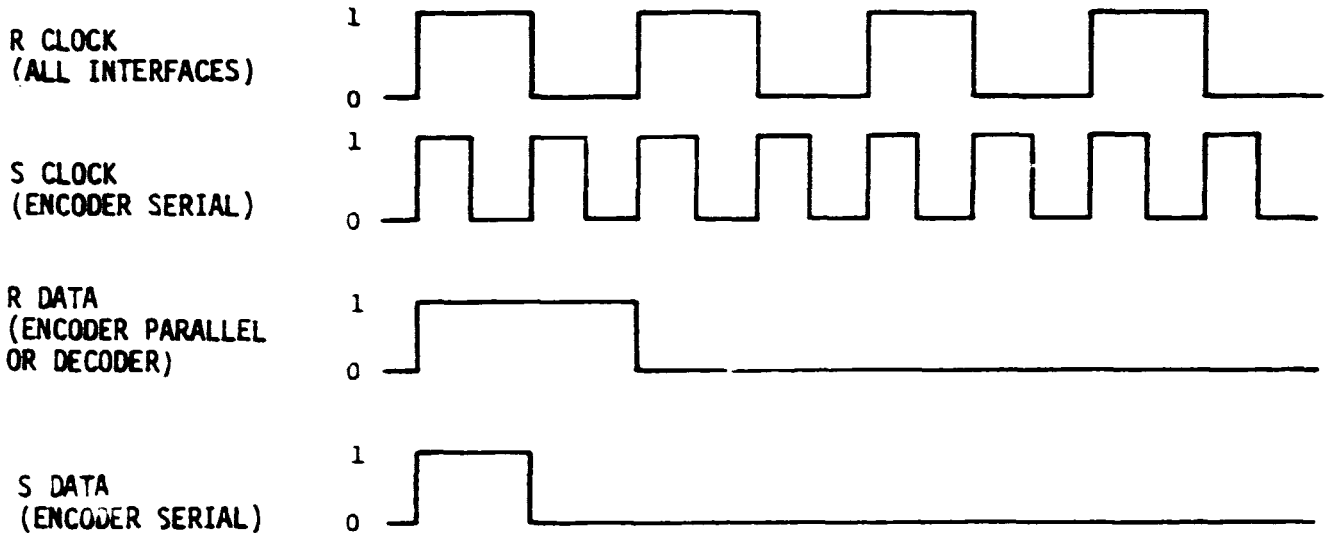

Figure 4-4. Transmitter Data and Clock Relationships, Rate 1/2 and 1/3

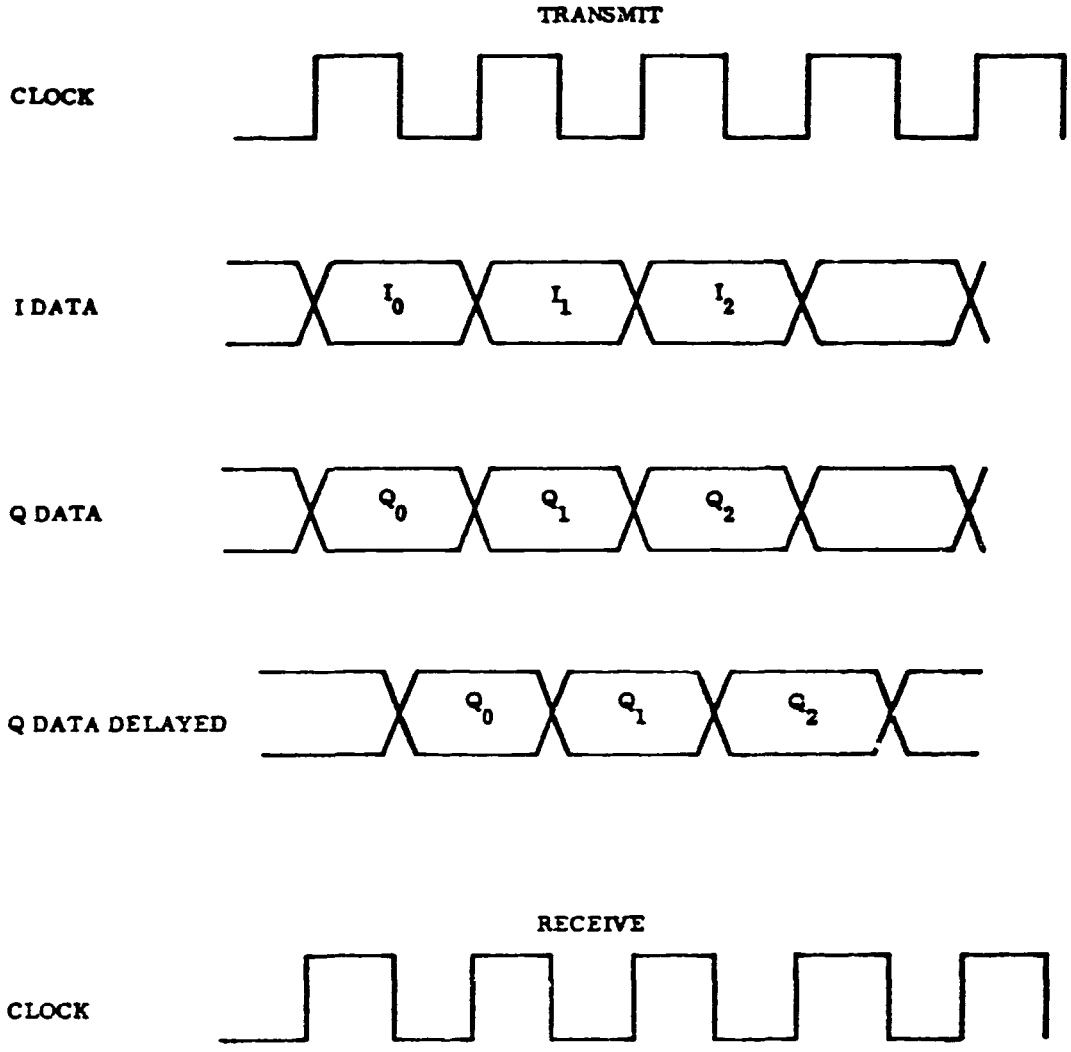

Figure 4-5. Offset (OQPSK) Data Format

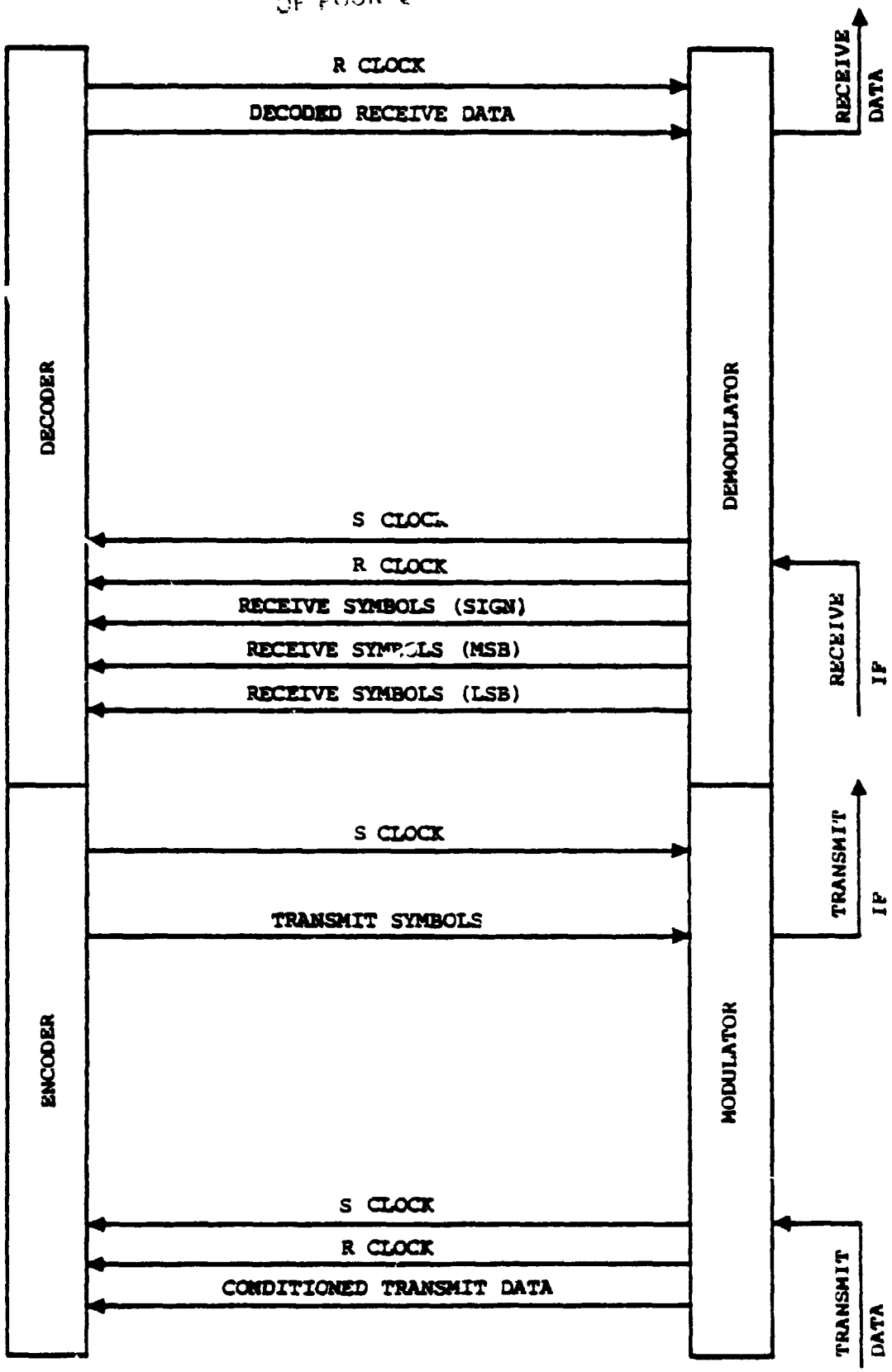

Figure 4-6. Interface for Serial Symbol Mode (BPSK)

4.5 PARALLEL SYMBOL STREAM (QPSK MODEM)

In the parallel symbol mode (rate 1/2 only), the encoder-decoder interfaces with a QPSK modem (figure 4-7). The modulator accepts the data, conditions it, and interfaces with the convolutional encoder. Two parallel encoded streams at rate R are returned to the modem. The receive modem output (either hard or soft decision) is formatted into two parallel symbol streams at rate R and is interfaced with the Viterbi decoder. The decoded data is returned to the demodulator for output conditioning. The appropriate clock accompanies data across all interfaces.

4.6 OFFSET PARALLEL SYMBOL STREAM (OQPSK MODEM)

In this parallel symbol mode (rate 1/2 only), the encoder-decoder interfaces with an offset QPSK modem in which the quadrature channels (I and Q) are offset in time, the Q channel trailing the I channel by 1/2 bit time. This offset is accomplished in the modulator after the encoding process. The interface arrangement is shown in figure 4-8. The modulator-encoder interfaces are similar to those in paragraph 4.5 except both the R and 2R clocks are present. The demodulator returns two parallel symbol streams, offset in time, to the decoder at rate R. The decoded data is returned to the demodulator for output conditioning. The appropriate clock accompanies data across all interfaces.

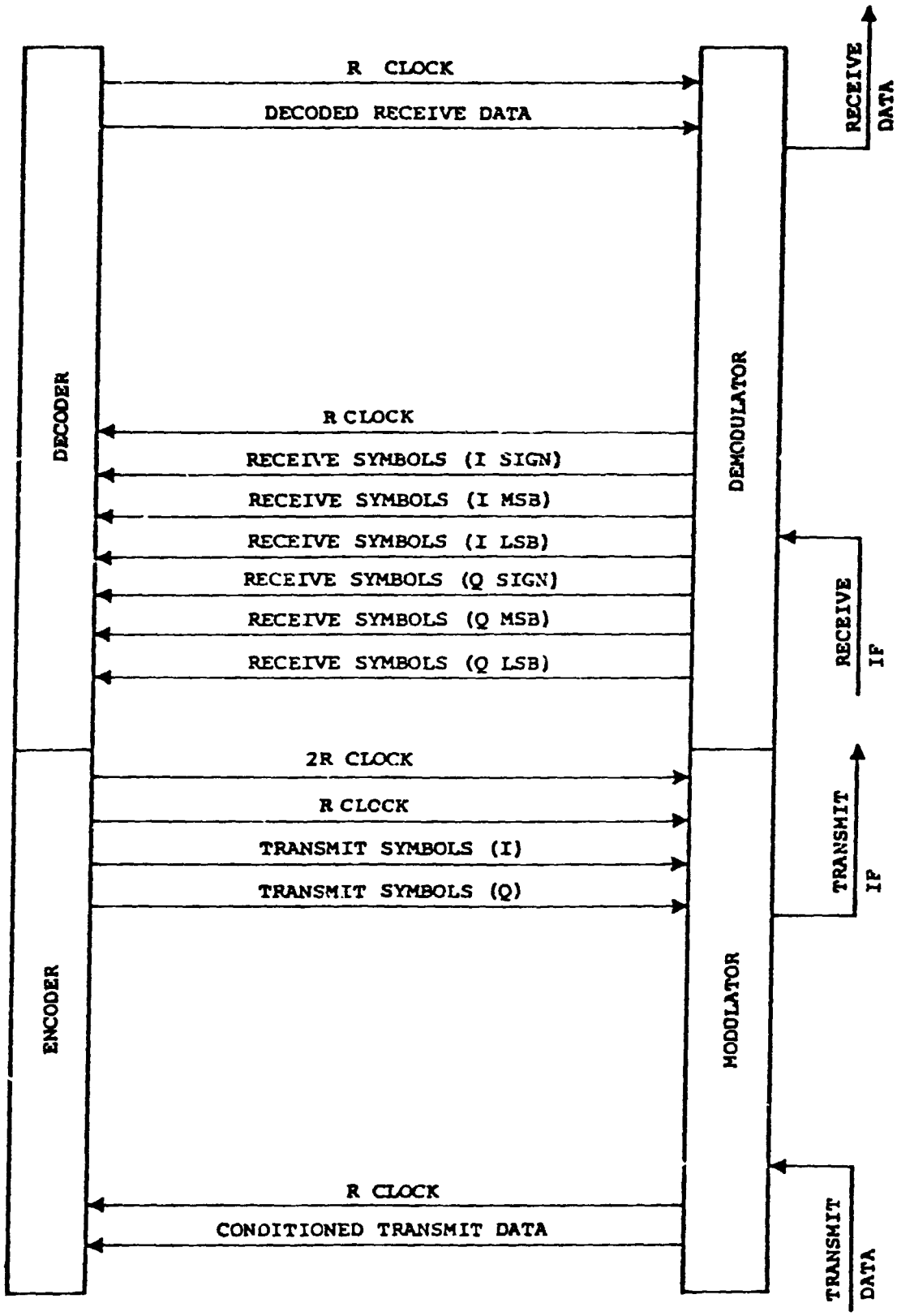

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Figure 4-7. Interface for Parallel Symbol Mode (QPSK)

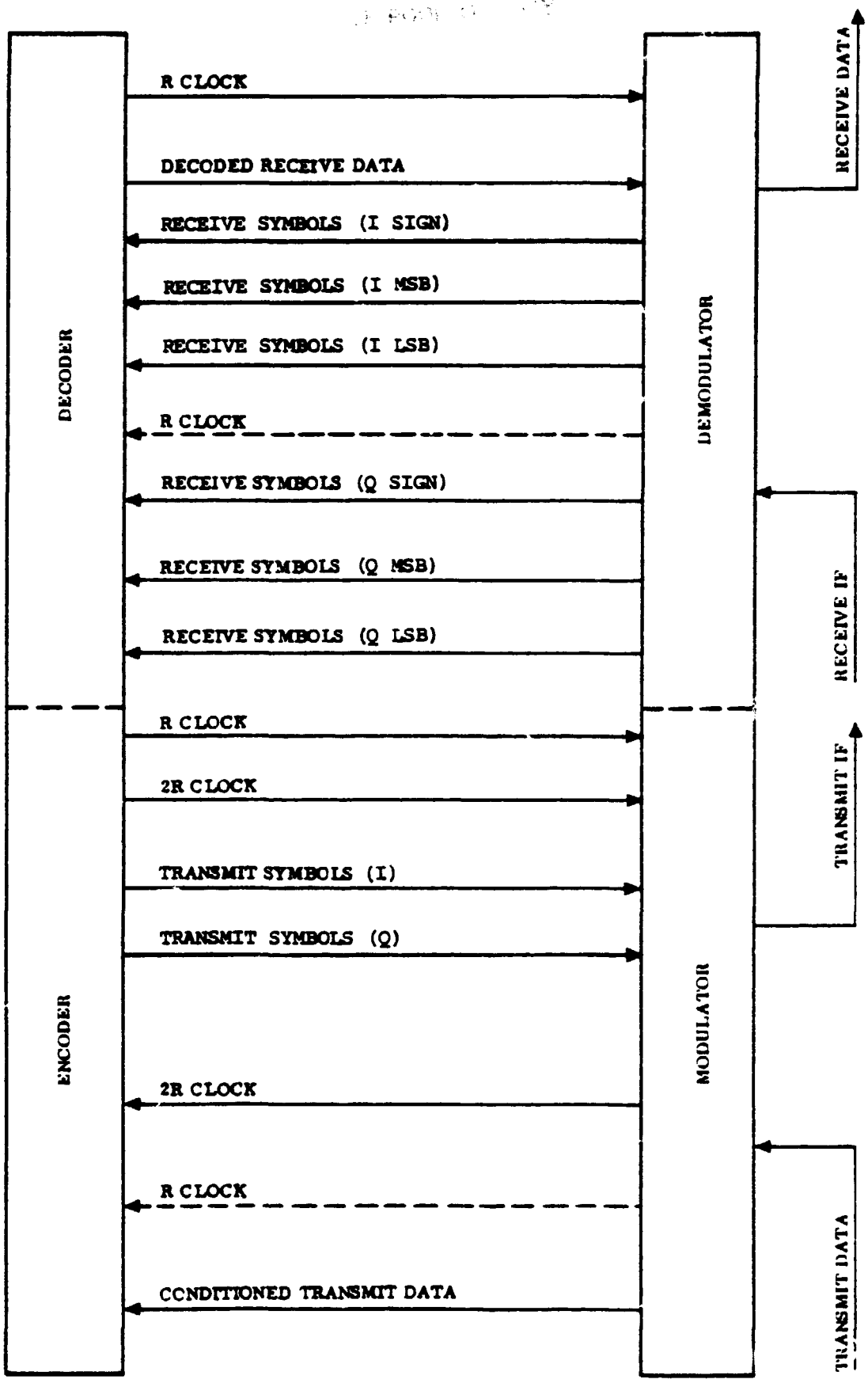

Figure 4-8. Interface for Parallel Symbol Mode (OQPSK)

4.7 ENCODER OPERATION

A rate 1/n, constraint length seven, convolutional encoder consists simply of a 7-stage shift register with n parity check networks, each connected to a distinct subset of the shift register outputs. An encoder is shown in block diagram form in figure 4-9. The n encoded output symbols are then formatted according to the particular mode of operation. The encoder is physically located on the input/output circuit card.

4.8 DECODER OPERATION

The method of decoding used in the equipment is an implementation of the Viterbi decoding algorithm. The decoder turns out to be much more complex than the associated encoder. Furthermore, the complexity of the decoder is dependent on the constraint length of the code; in this case, the constraint length is K = 7.

The algorithm calls for the performance of $2^{K-1} = 64$ arithmetic operations during each bit time, the output of each operation being a decision bit and a multibit number called a state metric.

The data input from the associated modem demodulator is reformatted into four multibit numbers called branch metrics, and are used, along with the stored metrics, during the arithmetic operations.

The 64 decisions are stored in a memory section called the path memory, and the 64 state metrics (M1 through M64) are stored in the metric memory. The state metrics are updated each bit time, but the decision bits are retained for a minimum of 32 bit times.

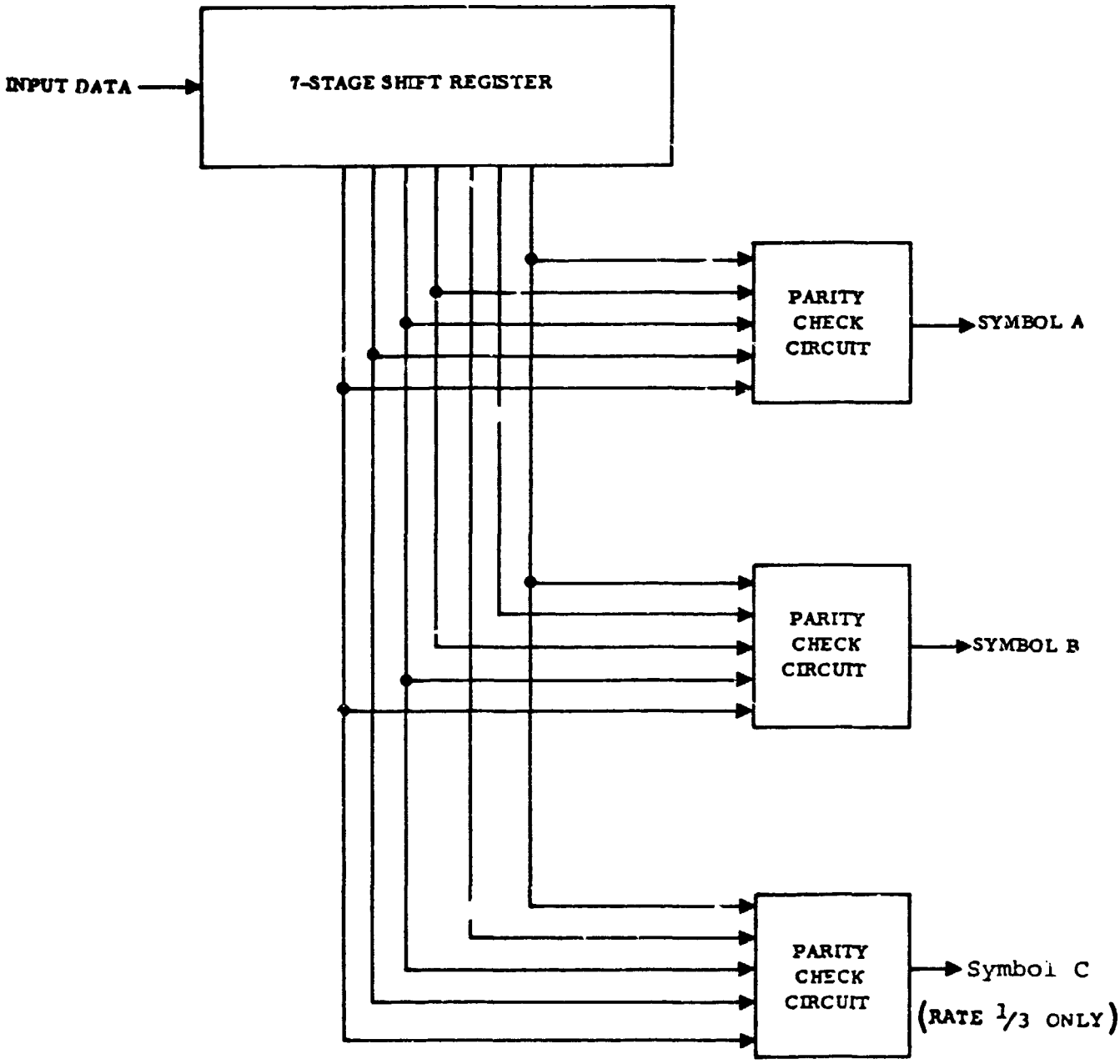

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Figure 4-9. B ock Diagram of Encoder on Input/Output Circuit Card Assembly

It is from the decision bits (D1 through D64) stored in the path memory that the decoded bit is selected, once each bit time.

The decision bits stored in the path memory are arranged in 64 groups called paths. One state metric is associated with each of the 64 paths. The decoding process then involves selecting the path with the best state metric (in this case, best means smallest valued), and the oldest decision bit associated with this best path is then selected as the decoded bit.

A block diagram of the decoder is shown in figure 4-10. The input section contains all the circuits necessary for formatting the data and forming the four branch metrics.

The arithmetic processor uses the four branch metrics and 64 state metrics to perform the required 64 operations, generating 64 updated state metrics which are restored in the metric memory. The arithmetic processor and the metric memory combine to make up the arithmetic section. The arithmetic processor also includes circuitry for determining the best state, i.e., the lowest valued state metric.

The 64 decision bits generated by the arithmetic processor are sent to the path memory where they are stored. The output section uses the data stored in the path memory and the best state output from the arithmetic processor to select the decoded output bit.

The input section and portions of the output section are located on the input/output circuit card A2. The remainder of the output

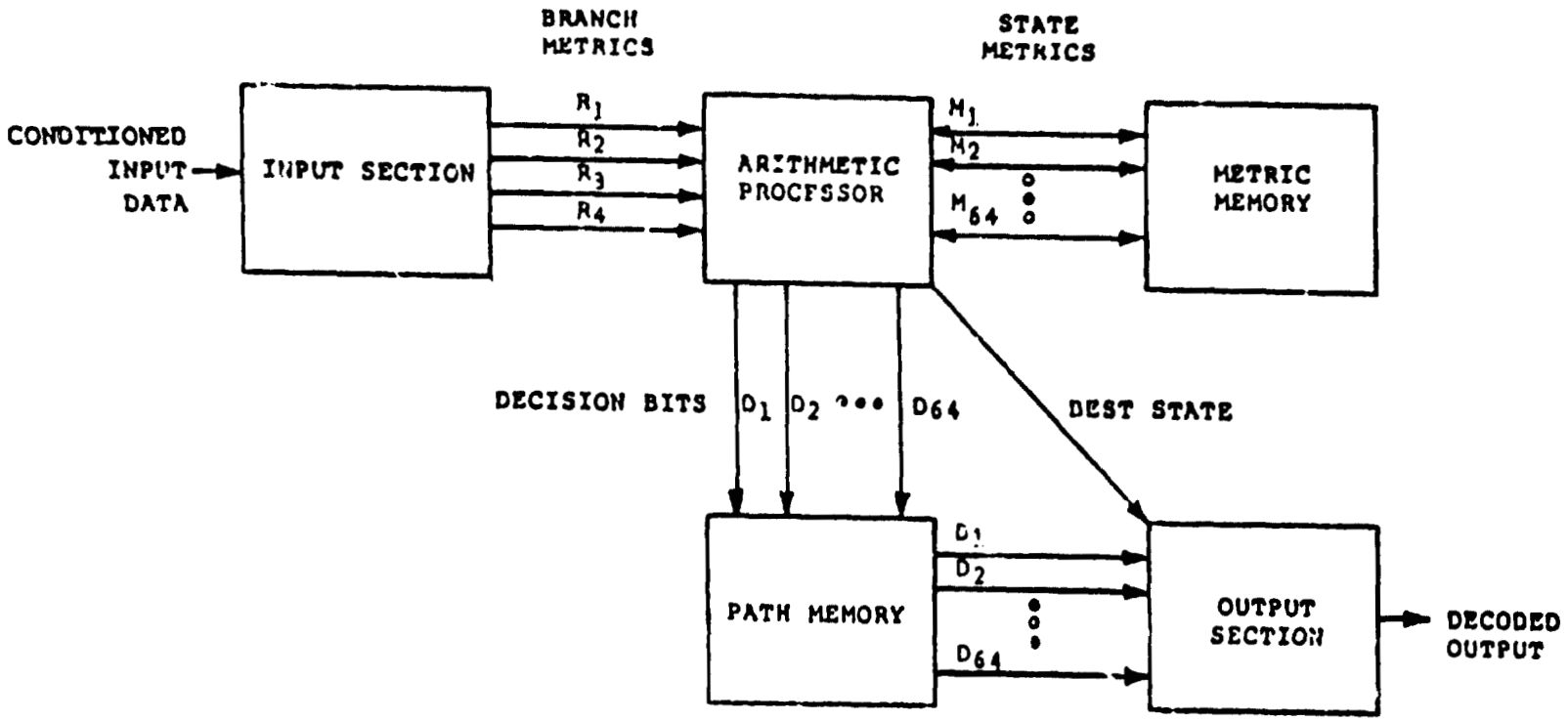


Figure 4-10. Block Diagram of the Decoder

section and the path memory are located on the path memory circuit card A3. The arithmetic section, consisting of the arithmetic processor and the metric memory are located on the arithmetic circuit card.

4.9 SELF-TEST FUNCTIONS

The on-line and off-line fault detectors and indicators using built-in test circuits are described in paragraphs 4.10 and 4.11.

4.10 ON-LINE MONITORING, TESTING, AND INDICATION

Refer to paragraph 3.2 for a description of the function of the on-line fault indicator. The on-line monitoring consists of both static and dynamic testing.

The on-line dynamic test circuits consist of the following:

1. Encoder fault detector
2. Decoder fault detector
3. Error counter, which drives the front panel ERROR RATE display
4. Clock fault detector, which generates a fault signal when a clock signal is interrupted.

An on-line test mode, called the LINK TEST, is provided to facilitate testing of complete communication links. The built-in pseudo-noise generator is used as the data input to the encoder; otherwise the encoder-decoder operates in its normal on-line mode. At the decoder, since the data sequence is known, both the decoder output error rate and the channel error rate can be measured using the procedures of paragraph 3.6. The procedures for entering the LINK TEST mode are described in paragraph 3.5.

4.11 OFF-LINE MONITORING AND INDICATION

The off-line tests consist of fault isolation and loop-back tests. The built-in test equipment for performing these tests includes a pseudo-noise data generator, error detector, and a digital noise generator. A microprogrammed processor controls the built-in test circuits in the fault isolation procedure.

The fault isolation test detects a go or no-go condition. When the MODE switch is in the OFF-LINE TEST position and the TEST pushbutton is depressed, the microprogrammed processor initiates a series of tests which provide a go or no-go indication. If a no-go condition exists, the FAULT indicator is illuminated. These tests do not, of course, detect every possible fault. The tests are designed to isolate those faults which are most likely to occur in the encoder-decoder. The test program includes a BITE self-test which inserts predetermined faults into the encoder-decoder. A momentary illumination of the FAULT indicator, shortly after cycling the TEST pushbutton, is proper and indicates that the self-test circuits have detected the inserted fault. After detection, these faults are removed and a steady illumination of the FAULT indicator signals a true fault.

The loop-back test (figure 4-11) is the last step of the off-line test sequence and is automatically enabled after the fault isolation procedure is completed. An internal oscillator provides the clock source and the pseudo-noise generator output is used as the encoder data input. The encoded output is passed to the digital noise generator which simulates the channel noise and puts out a signal which simulates the soft decision modem

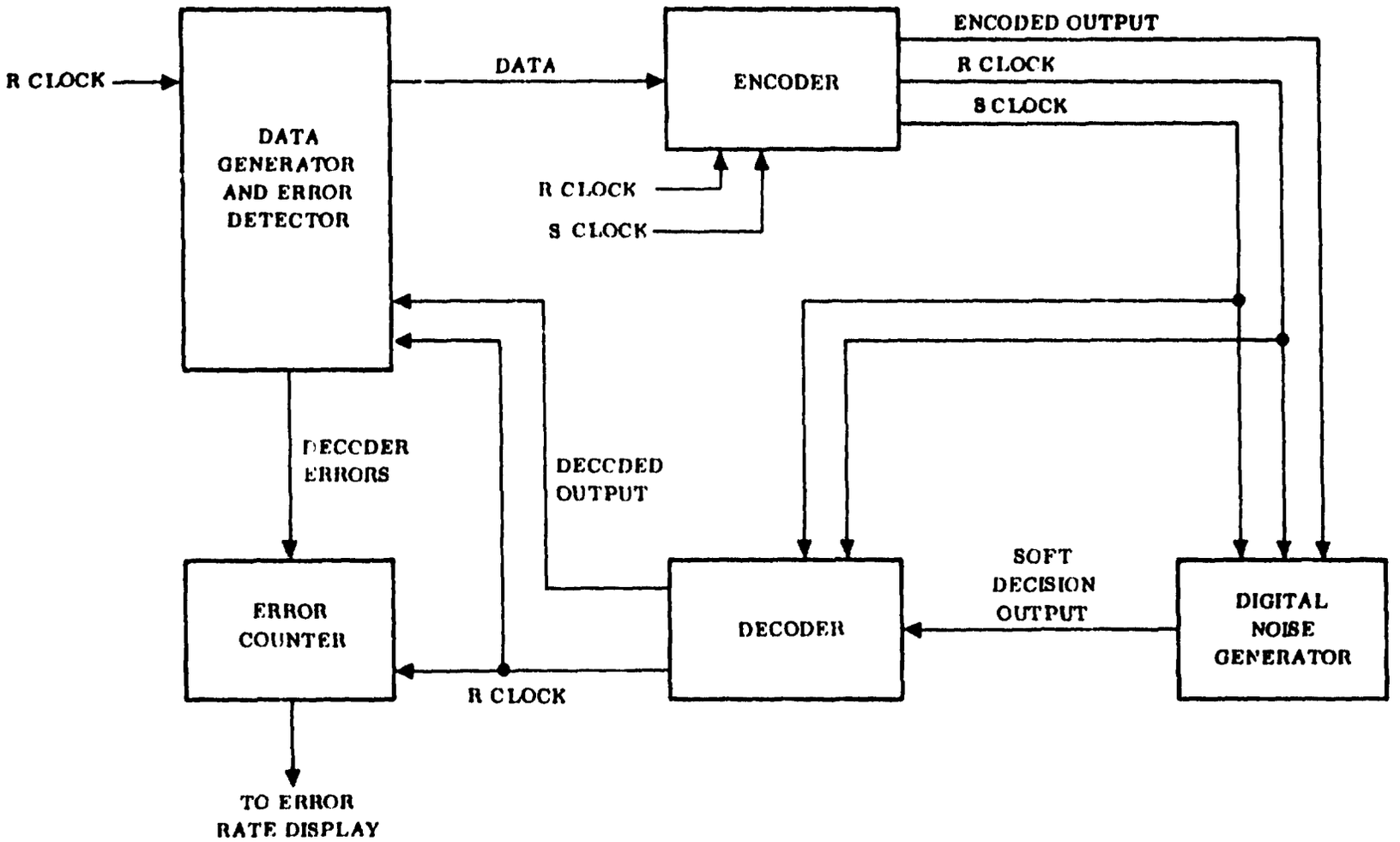


Figure 4-11. Loop-Back Test Mode

output. This corrupted version of the encoder output is then fed to the decoder. The ERROR RATE counter and display can now be used to measure either the simulated channel error rate or decoder output error rate. (Refer to paragraph 3.6.) The channel error rate should read approximately 0.050 and the output error rate should be less than 0.00006.

SECTION 5

MAINTENANCE INSTRUCTIONS

5.1 GENERAL

This chapter provides preventive and corrective maintenance instructions for the encoder-decoder. It lists tools, test equipment, and materials needed to troubleshoot the encoder-decoder, trace faults to chassis mounted discrete parts, and replace defective circuit card assemblies and chassis mounted discrete parts. Maintenance inspection and repair procedures in this chapter are for those parts which may be replaced at the on-site level of maintenance.

Tools, test equipment, and materials required for maintaining, troubleshooting, and repairing the encoder-decoder are listed in table 5-1.

5.2 PREVENTIVE MAINTENANCE

To ensure that the encoder-decoder is always ready for operation, it must be inspected systematically so that defects may be discovered and corrected before they result in serious damage or failure. Recommended preventive maintenance checks and services to be performed are listed in table 5-2. Defects discovered during operation of the unit should be noted for future correction to be made as soon as operation has ceased. Operation should be stopped immediately if a deficiency is noted during operation which would damage the equipment.

Table 5-1. Tools, Test Equipment, and Materials

Item	Description
Tool kit	Common electronic repair tools
Multimeter	Hewlett-Packard HP4106, or equivalent
Trichloroethane	
Cleaning cloths	
Brush	Soft bristle
Grease	MIL-G-23827, or equivalent
Loctite	Grade HV #77 (MIL-S-22473)
Wire	Hookup, AWG #22 (MS20995C20)

Table 5-2. Preventive Maintenance Checks and Services

ITEM TO BE CHECKED	PROCEDURE	SCHEDULE/ACTION
Encoder-Decoder	Check equipment for cleanliness.	Daily/Refer to paragraph 5.2.1 for cleaning instructions.
Switches	Check mechanical action for smoothness and positive detent action.	Daily/Refer to removal and replacement (paragraph 5.3.2).
Fan	Check that fan is operating by sensing airflow.	Each time equipment is energized/Ref to troubleshooti (paragraph 5.3.1).
Cables and Connectors	Check all interconnecting cables and connectors for cracks and breaks. Tighten all connectors.	Weekly/Refer to paragraph 2.1.
Off-line test	Perform OFF-LINE TEST.	Daily/Refer to paragraph 3.4.

5.2.1 CLEANING

Perform cleaning procedures as follows:

WARNING

The fumes of trichloroethane are toxic. Provide thorough ventilation whenever used. DO NOT USE NEAR AN OPEN FLAME. Trichloroethane is not flammable, but exposure of the fumes to an open flame or hot metal forms toxic phosgene gas.

CAUTION

- Do not allow trichloroethane to enter thumbwheel switches.

- Do not use on or allow trichloroethane to touch circuit card assemblies. Trichloroethane will damage the conformal coating on these assemblies.

1. Clean exterior surfaces with a clean, soft, lint-free cloth.

2. Clean areas around switches and indicators with a soft brush.

3. To remove grease, fungus, or corrosion, use a cloth dampened in trichloroethane.

5.3 CORRECTIVE MAINTENANCE

5.3.1 TROUBLESHOOTING

This section contains troubleshooting procedures (table 5-3) to isolate a fault in the encoder-decoder to a defective circuit card assembly or part. Test points used during troubleshooting are shown in figure 5-1. Most encoder-decoder faults will be quickly isolated by use of the OFF-LINE TEST method and the multimeter (paragraph 3.4). When the use of the multimeter is required for fault isolation, the required meter indications are shown in the troubleshooting chart in table 5-3. Ensure that the desired programmable installation options are installed. (See paragraphs 2.2.4 through 2.2.4.8.)

5.3.2 REMOVAL AND REPLACEMENT PROCEDURES

When trouble has been localized to a circuit card assembly or part, the defective part should be removed and replaced, as described in the following paragraphs.

5.3.2.1 FUSE - The fuseholder is mounted on the rear panel (figure 1-3). To remove and replace the fuse, proceed as follows:

1. Remove the fuseholder cap, and pull the defective fuse out of the cap.
2. Push the replacement fuse into the fuseholder cap until it seats properly.
3. Replace the cap in its receptacle and turn to lock.

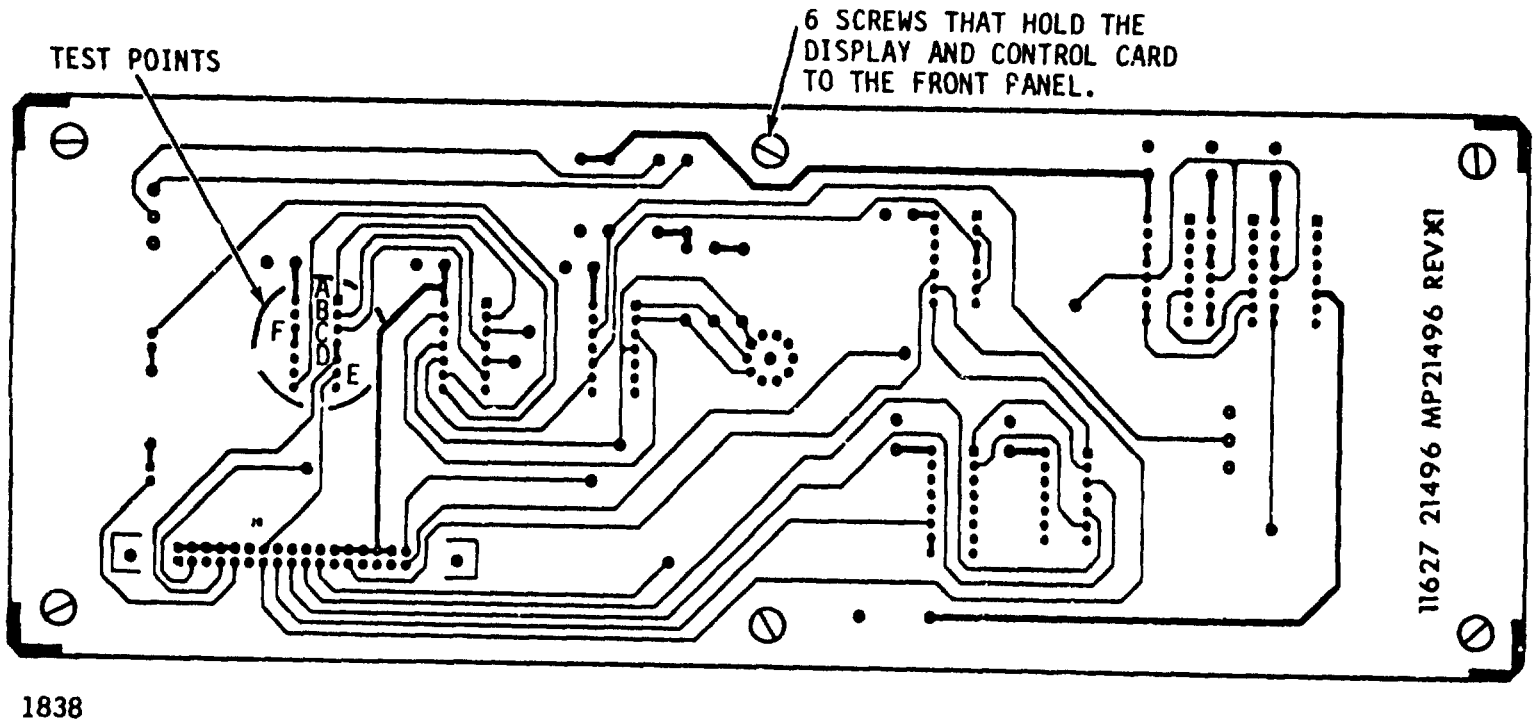


Figure 5-1. Display and Control Board (Rear View), Showing Troubleshooting Test Points

Table 5-3. Troubleshooting Chart

Item No.	Symptom	Probable Cause	Corrective Action
1	When POWER switch is set to ON, fan does not start and POWER indicator does not illuminate.	a. Blown fuse	a. Check blown fuse indicator. If illuminated, replace fuse (paragraph 5.3.2.1).
		b. Primary power is absent.	b. Check connector at source input and cable connection at rear of encoder-decoder.
		c. Defective primary power cable assembly.	c. Check continuity of cable and replace if defective.
2	When POWER switch is set to ON, fan does not start, but POWER indicator illuminates.	a. Defective fan	a. Check for 110 Vdc at terminals of fan. If voltage is present, replace fan (paragraph 5.3.2.2).
3	When POWER switch is set to ON, POWER indicator does not illuminate, but fan starts.	a. V_{CC} to ground short on one or more of the circuit card assemblies.	a. Turn POWER off. Remove a circuit card. Turn POWER on. If POWER indicator lights, replace the card removed. If not, repeat for all circuit card assemblies.

Table 5-3. Troubleshooting Chart (Continued)

Item No.	Symptom	Probable Cause	Corrective Action
3	Continued	b. Defective backplane.	b. Power down. With all CCA's removed make continuity check from V_{CC} to ground terminals on backplane. Replace if shorted.
		c. Defective power supply.	c. Replace power supply.
4	FAULT Indicator illuminates	a. Fault in one or more circuit cards.	Probe points A-F on display and control board, as shown in figure 5-1. Fault is indicated by the presence of a logic zero at any of these points. Proceed to 4A, 4B, 4C, 4D, 4E or 4F as indicated. If none are logic zero, replace display and control card.
4A	Pin A shows FAULT	a. Arithmetic card improperly seated or defective.	a. Reseat or replace Arithmetic card as necessary.
4B	Pin B shows FAULT	a. I/O card improperly seated or or defective.	a. Reseat or replace I/O card as necessary.

Table 5-3. Troubleshooting Chart (Continued)

Item No.	Symptom	Probable Cause	Corrective Action
4C	Pin C shows FAULT	a. Path memory card improperly seated or defective.	a. Reseat or replace path memory card as necessary.
4D	Pin D shows FAULT	a. Encoder is malfunctioning.	a. Replace I/O card.
4E	Pin E shows FAULT	a. Decoder FAULT	a. Perform OFF-LINE TEST and take corrective action as indicated by state of pins A, B and C.
4F	Pin F shows FAULT	a. Clock fault due to improper connection.	a. Verify presence of encoder clock inputs and decoder clock inputs.
		b. Clock fault due to circuit card failure.	b. Perform OFF-LINE TEST and take corrective action as indicated by status of pins A, B, and C.
5	STATUS SYNC indicator does not illuminate, and FAULT does not illuminate during off-line tests.	a. Improperly seated or defective circuit card.	a. Reseat circuit cards. If fault remains, replace circuit cards one at a time.

Table 5-3. Troubleshooting Chart (Continued)

Item No.	Symptom	Probable Cause	Corrective Action
5	Continued	b. Defective I/O cable.	b. Perform continuity check on I/O cable and replace if faulty.
		c. Defective display and control circuit card.	c. Replace display and control circuit card.
		d. Defective backplane circuit card.	d. Replace backplane circuit card.

5.3.2.2 PLUG-IN CIRCUIT CARD ASSEMBLIES - To remove and replace plug-in circuit card assemblies, proceed as follows:

1. Release the two front panel fasteners (figure 1-1) and lower the panel.

2. Identify the circuit card assembly (figure 1-2) to be removed. To remove the input/output circuit card assembly card (card 3), disconnect the flat cable connector.

3. Unseat the circuit card from the receptacle by first pulling outward on the circuit card ejector tabs. After unseating the circuit card, return the ejectors to their original position.

4. Carefully pull the circuit card straight out of the chassis.

5. Lay the card on a clean workbench with the component side up. Handle the card at the edges.

6. Insert the replacement circuit card assembly in the guide slots and carefully press straight in until its connector is fully engaged in the receptacle. Secure the front panel fasteners.

5.3.2.3 REPLACEMENT OF DISPLAY AND CONTROL CIRCUIT CARD - To remove and replace the display and control circuit card, proceed as follows:

1. Remove dress nuts and washers from all front panel toggle switches except the POWER switch. Loosen the setscrew on the MODE switch knob and remove the knob and dress nut.

2. Open the front panel, and remove cables from connector J8.

3. Unsolder the FAULT and SYNC LED leads at the rear of the Display and Control Card.

4. Remove the six circuit card mounting screws, flat washers, and lockwashers (figure 5-1). Remove the

circuit card from the front panel. The FAULT and SYNC LEDs will remain with the front panel.

5. Position the replacement circuit card carefully over the LED leads and centered over the standoff holes from which the six screws and washers were removed in 3.

6. Install the replacement circuit card using the six screws, and solder the LED leads to the card. Connect the cable removed in step 2 to J8.

7. Close and secure the front panel. Replace the toggle switch washers and dress nuts and the MODE switch knob and dress nut removed in step 1.

5.3.2.4 REPLACEMENT OF 5-VOLT POWER SUPPLY - To remove and replace the 5 volt power supply, proceed as follows:

1. Single screws at the rear of the top and bottom covers hold the covers to the chassis. Remove the screws and slide off the covers.

2. Remove the rear panel by removing the four corner screws (figure 1-3).

3. Remove the barrier strips on the power supply terminal boards. Tag and remove the wires at the terminal boards.

4. Four screws on the chassis bottom hold the power supply to the chassis. Remove these screws and lift the power supply from the chassis.

5. Lower the replacement power supply into the chassis and attach the power supply, using the four screws removed in step 4.

6. Attach the wires at the terminal boards. Attach the barrier strips to the terminal boards.

7. Attach the rear panel to the chassis using the four screws removed in step 2.

8. Slide on the top and bottom covers and attach the covers using the screws removed in step 1.

5.3.2.5 FAN - To remove and replace the fan, proceed as follows:

1. Single screws at the rear of the top and bottom covers hold the covers to the chassis. Remove the screws and slide off the covers.

2. Remove the finger guard on the fan by removing the four screws (figure 1-3).

3. Remove the fan wires.

4. Remove the four screws, eight washers, and four nuts that hold the fan to the chassis.

5. Attach the replacement fan to the chassis, using the hardware removed in step 4.

6. Attach the fan wires.

7. Attach the finger guard to the fan, using the four screws removed in step 2.

8. Slide on the top and bottom covers and attach, using the screws removed in step 1.

SECTION 6

LOGIC DIAGRAMS

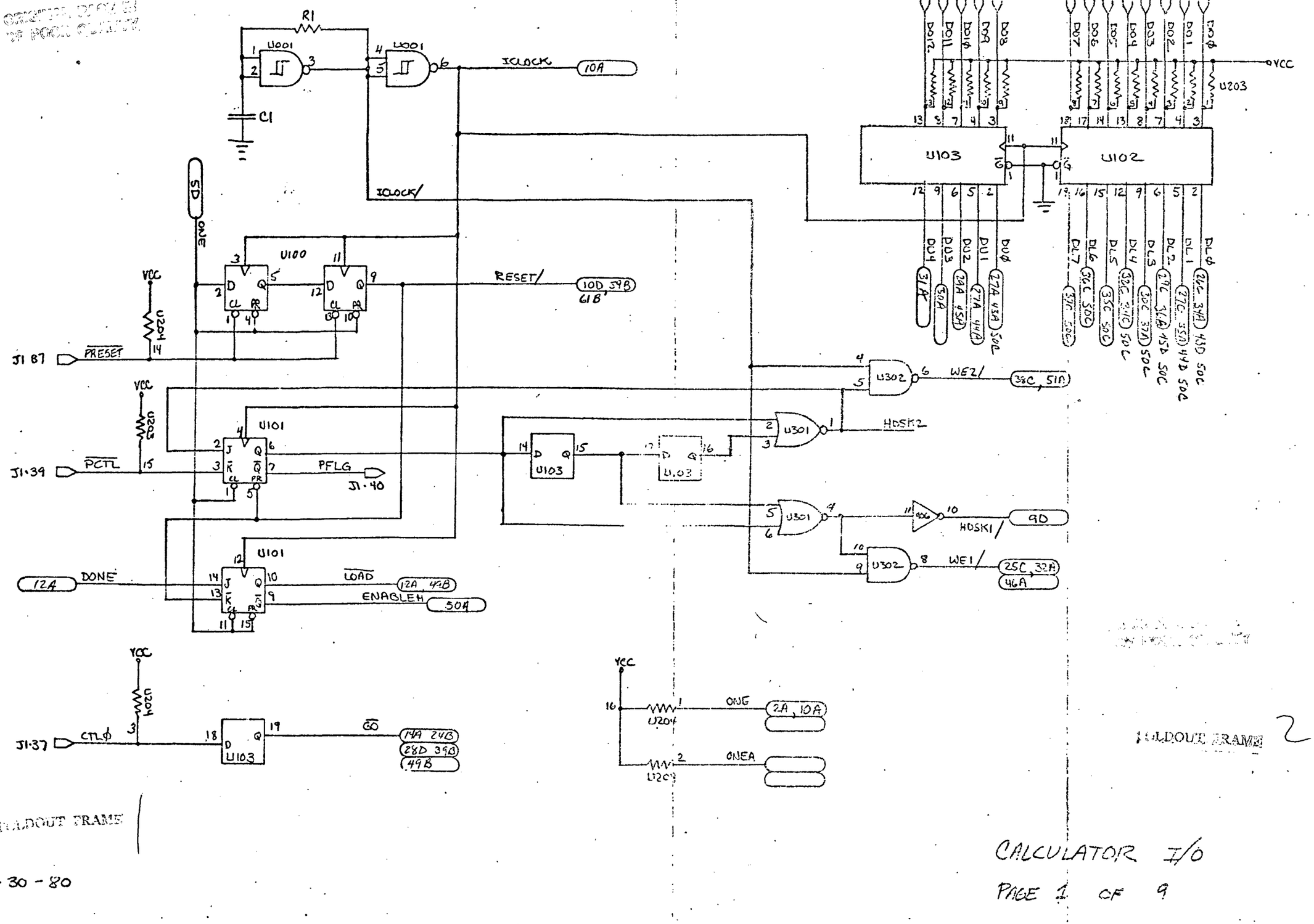
6.1 INTRODUCTION

This section contains logic diagrams of the Input/Output, Arithmetic, and Power Supply circuit cards.

6.2 LIST OF DRAWINGS

The following is a list of drawings contained in this section:

Drawing Number	Title
LD 21368	Input/Output CCA
LD 21369	Arithmetic CCA
LD 21493	Backplane CCA



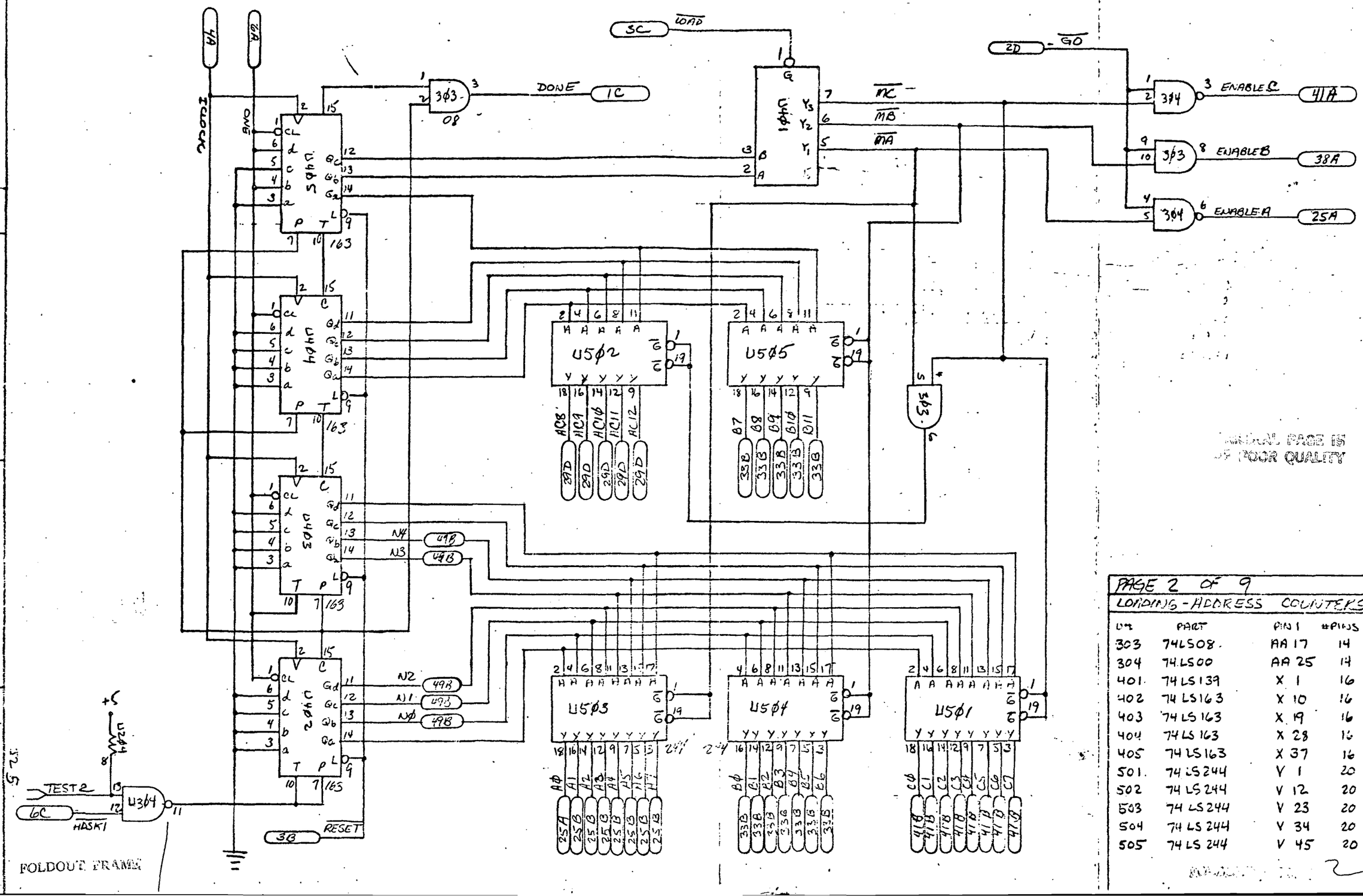
PALDOUT FRAME

PALDOUT FRAME 2

10-30-80

CALCULATOR I/O

PAGE 1 OF 9



PAGE 2 OF 9

LOADING - ADDRESS COUNTERS

U#	PART	PIN 1	#PINS	VCC	GND
303	74LS08	AA 17	14	14	7
304	74LS00	AA 25	14	14	7
401	74LS139	X 1	16	16	8
402	74LS163	X 10	16	16	8
403	74LS163	X 19	16	16	8
404	74LS163	X 28	16	16	8
405	74LS163	X 37	16	16	8
501	74LS244	V 1	20	20	10
502	74LS244	V 12	20	20	10
503	74LS244	V 23	20	20	10
504	74LS244	V 34	20	20	10
505	74LS244	V 45	20	20	10

74LS377

U209 U211 U210 U107 U207 U106 U108 U208

R7 R16 R4 R2 R19 R18 R13 R0 R5 R10 R14 R8

U304 74S00 U406 74S04 DRESET 63C

U306 U308 U308 U308 U307 U307 U307 U307 U308 U309 U306 U305 U309 U306 U309 U306 U305 74S86

DCLOCK1

U310

RDL-54-032

RNG1

$1 + x + x^3 + x^4 + x^{64}$

#1 RANDOM NUMBER GENERATOR

REVISION: 9-80

U008 U908 U808 U009 U909 U809 U709 U708

R1 R11 R7 R6 R9 R12 R5 R3

U018 U017 U016 DRESET

DCLOCK2

REVISION:
9-80

U606 U607 U608

R19 R18 R17 R16 R15 R14 R13 R12 → A7 A6 A5 A4 A3 A2 A1 A0 (25B 25B 25B 25B 25B 25B 25B 25A)

R11 R10 R9 R8 R7 R6 R5 R4 → B11 B10 B9 B8 B7 B6 B5 B4 (33B)

R3 R2 R1 R0 → B3 B2 B1 B0 (33B 33B 33B 33B)

600 DCLOCK1 GO 3D

— RNG2 —
$1 + x + x^{63}$

#2 RANDOM NUMBER GENERATOR

A B C D

ENABLE A

16A

4φ7 4φ6 4φ7

12D,24A Aφ

12D,24A A1 A2 A3 A4 A5 A6 A7

HC8 HC9 HC10 HC11 HC12

DUφ 8B DU1 DU2 DU3 DU4

WE1 6C

U9φ4 U7φ5 U8φ5 U9φ5 Uφφ5

U7φ3 U8φ3 U9φ3 U7φ4 U8φ4

DLφ DL1 DL2 DL3 DL4

8A 50B 7φ T1 T2 T3 T4 29D,50B

U6φ4 U6φ5

54B GATE 60D CLOCK1 3D 6Q 32C T4

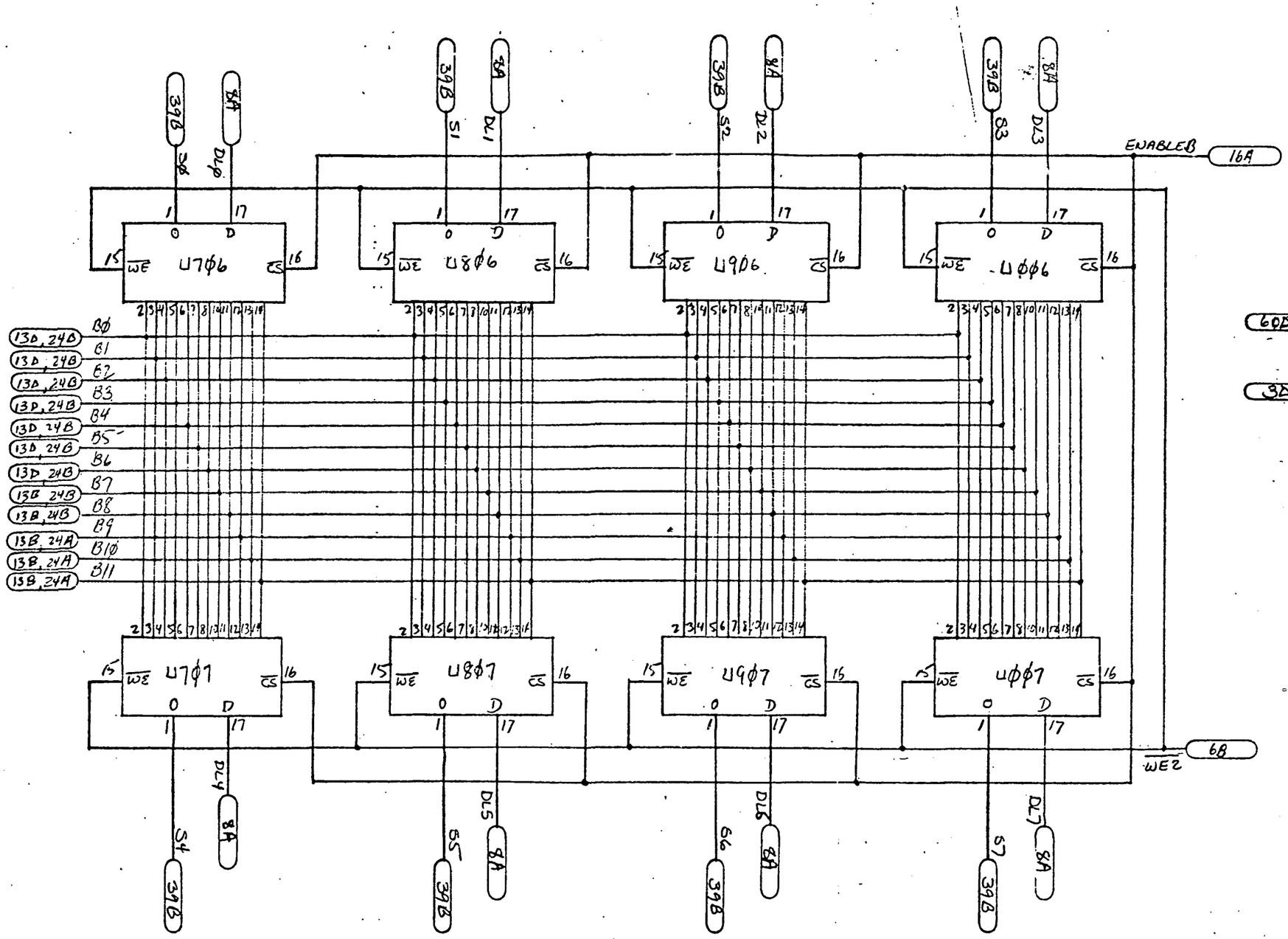
A08 HC9 HC10 HC11 HC12 12B,41B 12C,41B

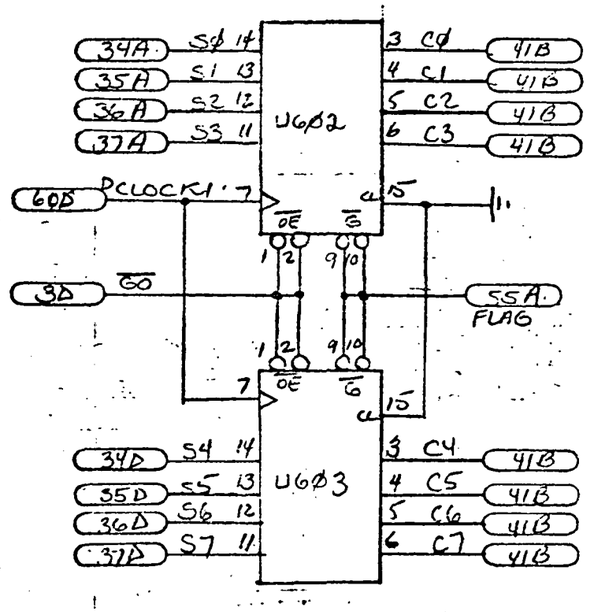
FOLDOUT FRAME

PAGE 5 OF 9

8K x 5 STATE MEMORY A

U#	PART	PIN 1	#PINS	VCC	GND
406	74LS04	X 46	14	14	7
407	74LS00	X 54	14	14	7
604	74LS173	T 28	16	16	8
703	93471	R 21	18	18	9
704	93471	R 31	18	18	9
705	93471	R 41	18	18	9
803	93471	P 21	18	18	9
804	93471	P 31	18	18	9
805	93471	P 41	18	18	9
903	93471	M 21	18	18	9
904	93471	M 31	18	18	9
905	93471	M 41	18	18	9
005	93471	K 41	18	18	9
605	74LS173	T 37	16	16	8

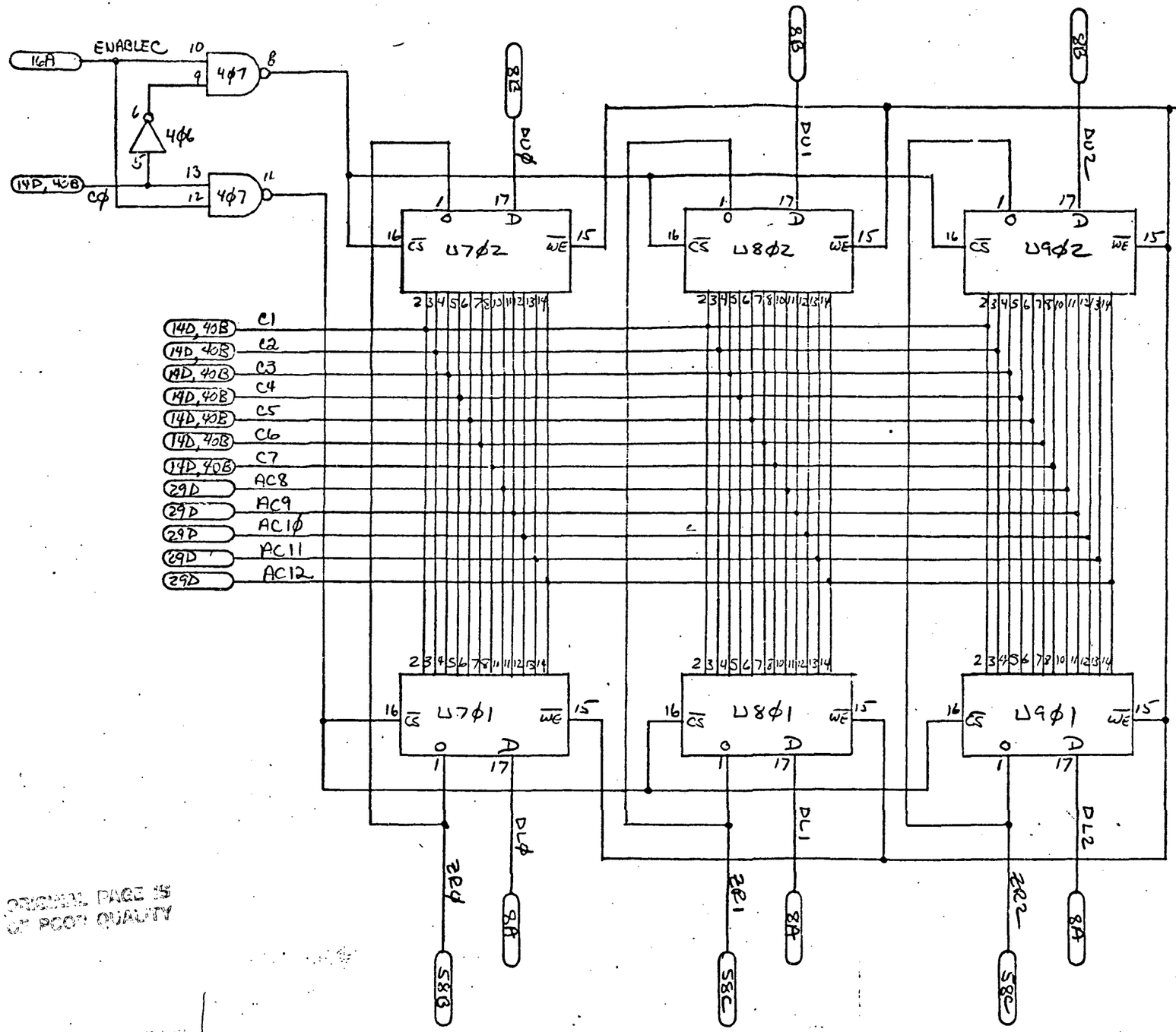




PAGE 6 OF 9

4K x 8 "REGION" MEMORY B

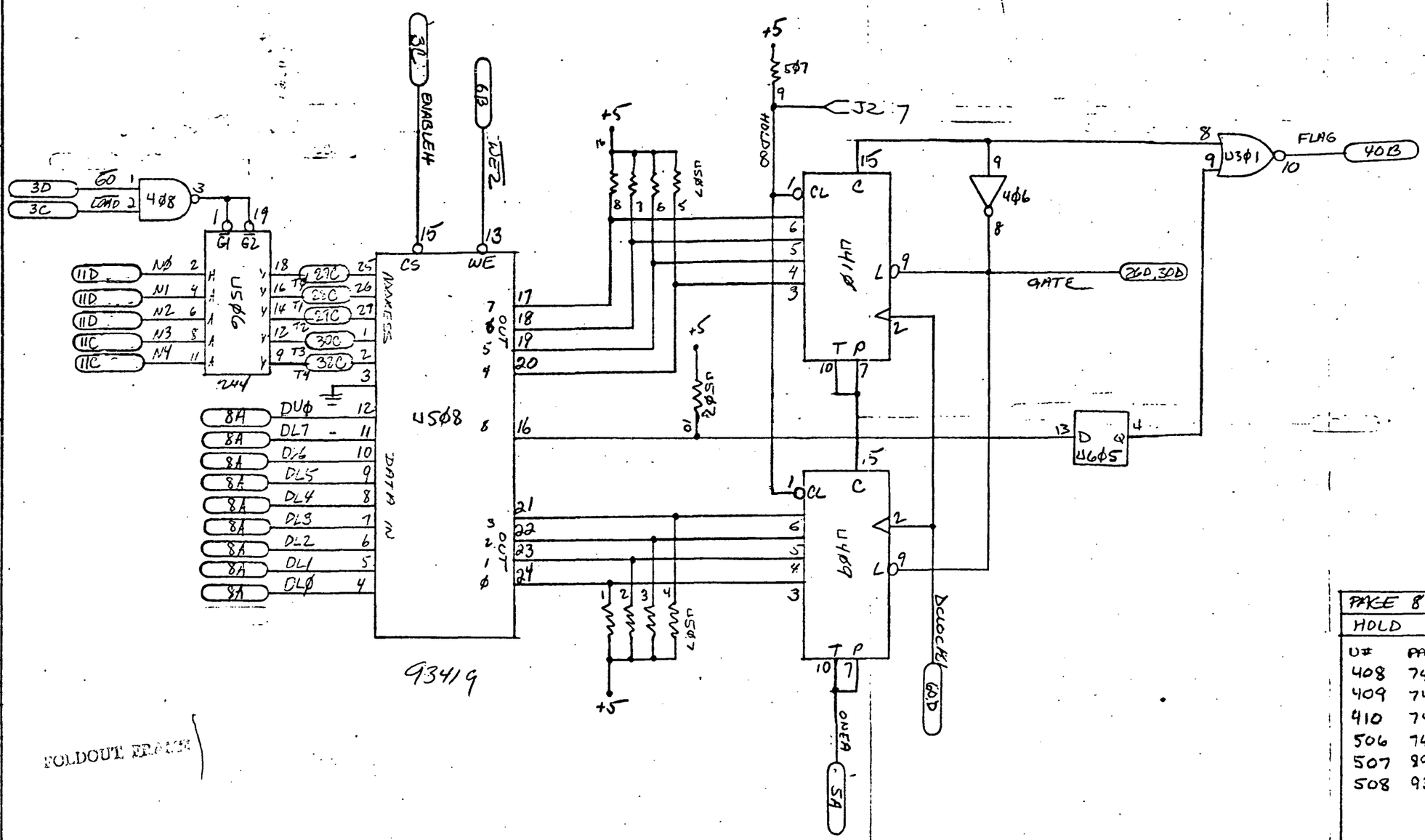
U#	PART	PIN 1	#PINS	VCC	GND
602	74LS173	T10	16	16	8
706	93471	R51	18	18	9
707	93471	R61	18	18	9
806	93471	P51	18	18	9
807	93471	P61	18	18	9
906	93471	M51	18	18	9
907	93471	M61	18	18	9
006	93471	K51	18	18	9
007	93471	K61	18	18	9
603	74LS173	T19	16	16	8



PAGE 7 OF 9

8K x 3 OUTPUT MEMORY C

U#	PART	PIN1	#PINS	VCC	GND
7φ1	93471	R 1	18	18	9
7φ2	93471	R 11	18	18	9
8φ1	93471	P 1	18	18	9
8φ2	93471	P 11	18	18	9
9φ1	93471	M 1	18	18	9
9φ2	93471	M 11	18	18	9



FOLDOUT FRAME

PAGE 8 OF 9					
HOLD STATE					
U#	PART	PIN 1	#PINS	VCC	GND
408	74LS00	X 62	14	14	7
409	74LS163	X 70	16	16	8
410	74LS163	X 79	16	16	8
506	74LS244	V 56	20	20	10
507	898-1-RIK	V 67	16	16	—
508	93419	V 79	28	28	14

A

B

C

D

U105

CLKINT
CLKINF
IN0T
IN0F
IN1T
IN1F
IN2T
IN2F

J2·2 (B1) BYPASS

+5

U601

U601

U104

CLKOUTT
CLKOUTF
1OUTT
1OUTF
2OUTT
2OUTF
3OUTT
3OUTF

43 RESET/

43D 2R0
44D 2R1
45D 2R2

5D ONEA

U206

U305

U305

U406

U202

U202

DRESET RNG1, 2

FOLDOUT FRAME

U201

INT
INF
CLKT
CLKF

U202

U302

U302

DCLOCK1 28D 39B 53D, RNG1, 22B

DCLOCK2 RNG2

BITSLIP

INVERT

U000

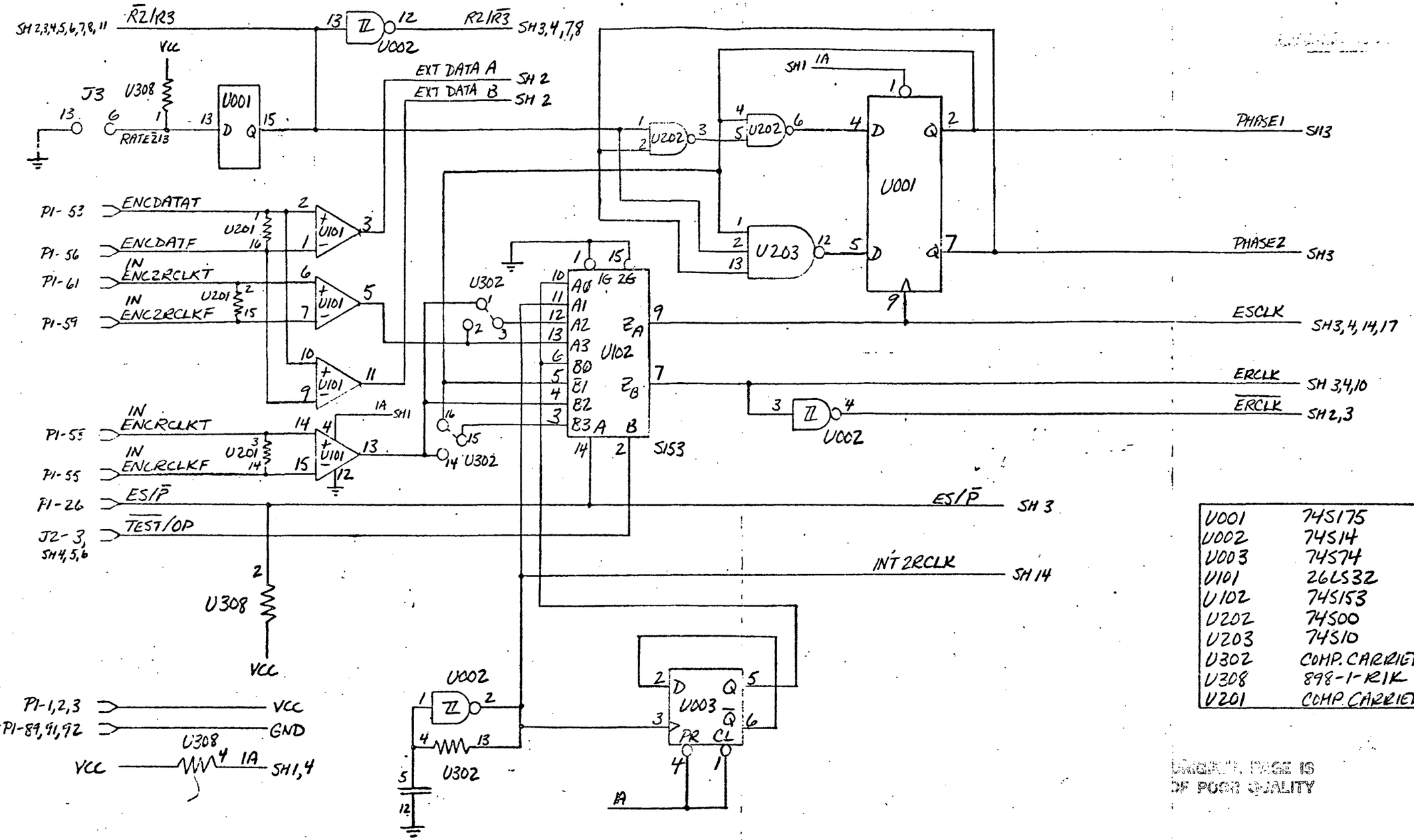
R2 R3 (S2)

R4 R5 (S3)

NC NO C

DATA PATH
PAGE 9 OF 9

11-3-80



U001	74S175
U002	74S14
U003	74S74
U101	26LS32
U102	74S153
U202	74S00
U203	74S10
U302	COMP. CARRIER
U308	898-1-R1K
U201	COMP. CARRIER

I10 BOARD	LD21368	SH1
ENCODER CLOCKS		

U004	825129
U005	825129
U006	74LS174
U103	74LS157
U104	74LS164
U105	74LS164
U204	74LS08
U205	74LS86
U206	74LS27
U207	74LS86
U308	898-1-R1K
U911	COMP. CARRIER
U912	96L02

SH2 1B

SH10 INT DATA

SH1 EXT DATA A

SH1 EXT DATA B

J2-1 DATA INT/EXT

U103

U308

VCC

U104

U105

U004

U005

U006

U205

U204

ERCLK

ENC DIFF

J3 2 17

U510

J3 18 1 REVERSE

PA SH3

PB SH3

PC SH3

U205 U205 U207

U206

FOLDOUT FRAME 2

ORIGINAL PAGE IS OF POOR QUALITY

U912

ENC FLT J2-4

U911

VCC U308 5 1B SH2,3

FOLDOUT FRAME 1

ORIGINAL PAGE IS OF POOR QUALITY

I/O BOARD SH 2

ENCODER

SH1 $\overline{ERCLK}$ 12 — U202 — S00 — 11

SH1 R2/$\overline{R3}$ 13 — U202

SH1 $\overline{R2}$/R3 9 — U202 — S00 — 8

10 — U202

(REGISTER U001 CLOCKED BY ESCLK)

U001: 12 D, 11 $\overline{Q}$

1, 2 — U208 — S00 — 3

SH1 ES/$\overline{P}$ 4

ENC INV 5 — U208 — 6

3, 2 — U108 — S02 — 1

9 U308 — VCC

5, 4 — U207 — 6

9, 10 — U207 — 8

J3: 16, 3

LS153

SH2 PC 6

SH2 PA 3

SH2 PB 4

U106: Aϕ, A3, A2, 1G, 2G, B, A; 4A = 7

1G = 1, 2G = 15

SH1 PHASE2 2

SH1 PHASE1 9 — U208 — 8 — 10

SH1 ES/$\overline{P}$

SH2 1B

SH1 ESCLK

U107: 4 PR, 1 CL, 2 D, 3, 11, 12 D, 10 PR, 13 CL; Q 5, $\overline{Q}$ 6, $\overline{Q}$ 8, Q 9

SH2 1B — U401: 4, 2, 1, 3, 12

SH1 ERCLK

OUT ENCRCLKT — P1-52

OUT ENCRCLKF — P1-50

SH1 ESCLK — U401: 6, 7, 5

OUT ENC2RCLKT — P1-49

OUT ENC2RCLKF — P1-47

S74

U401: 10, 11

ENCIOUTT — P1-43

ENCIOUTF — P1-41

U401: 14, 13

ENCQOUTT — P1-44

ENCQOUTF — P1-46

PCA — SH14

PCB — SH14

U001	74S175
U106	74LS153
U107	74S74
U108	74S02
U202	74S00
U207	74LS86
U208	74S00
U308	898-1-R1K
U401	26LS31

IO BOARD SH 3

ENCODED DATA FORMATTING

U002	74S14
U203	74S10
U301	26LS32
U303	74S175
U304	74S37
U308	8T8-1-121K
U402	74128
U403	74S153
U509	74LS08
U704	74S157
U805	74LS00

SH1 1A

SH 1 R2/R3

U805

U304

U203

U303

INTCLK → P1-19

SH1 1A

P1-34 DEC2RCLKT
P1-32 DEC2RCLKF
P1-29 DECRCLKT
P1-31 DECRCLKF

U201 4 13
U201 5 12

U301

S153

U403

U704

U304 S37

DSCLK → SH6
DSCLK → SH5
DRCLK → SH6,7,8,11,12,14,17
DRCLK → SH6, 9,11,12,13
P1-68

LS128

U402

DRCLK1 → SH9

SH1,3,14 ESCLK
SH 1,10 ERCLK
SH1, J2-3 TEST/OP
P1-28 DS/P

SH8 INTLVR IN

U002

SERIPAR SH16,5

U308

Vcc

SH1 R2/R3

U509

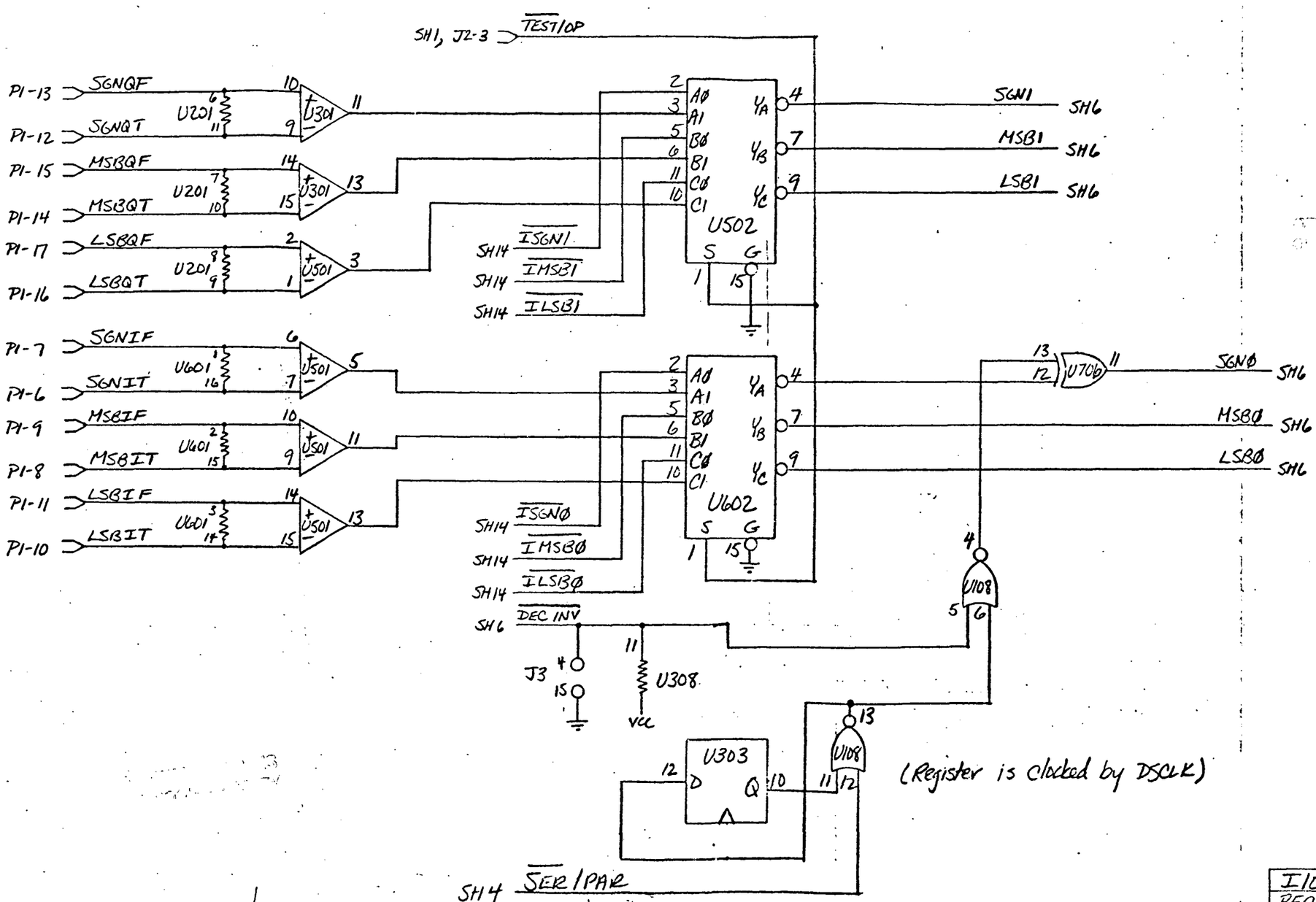
R2SYNC → SH6

FOLDOUT FRAME

FOLDOUT FRAME

I/O BOARD SH 4
DECODER CLOCKS

L. 1108	74S02
L 1301	26LS32
L 1303	74S175
L 1308	898-1-R1K
L 1501	26LS32
L 1502	74LS158
L 1602	74LS158
L 1706	74LS86



FOLDOUT FRAME

FOLDOUT FRAME

I/O BOARD SH 5

RECIEVE INF JT SYMBOLS FOR DECODE

SH5

FOLDOUT FRAME

SH 4 $\overline{DSCLK}$

SH5 SGNØ

SH5 MSBØ

SH5 LSBØ

U503 (CP, DA, DB, DC, CL; QA, QB, QC)

U504 (AØ, AI, BØ, BI, CØ, CI, E; YA, YB, YC)

SH8 IE

SH8 SYNC2

SH1 $\overline{R2IR3}$

SH4 R2SYNC

U404

PI-25 OFQPSK/$\overline{QPSK}$

SH1, J2-3 $\overline{TEST/OP}$ 11

U302

U308

VCC

SH8 $\overline{HARD/SOFT}$

SH4 DRCLK

SH5 SGNI

SH5 MSBI

SH5 LSBI

U603 (CP, CLR, DA, DB, DC, DD; QA, QB, QC, QD)

U604 (AØ, AI, BØ, BI, CØ, CI, E; YA, YB, YC)

PI-79 NORM

NORMALIZE SH 8, 15, 17

SH 4 $\overline{SER/PAR}$

PI-67 DATA OUT

U405 (CLR, RS, A, B, C; QA, QB, QC, QD, SI, SØ)

U306

U505 (CLR, RS, A, B, C; QA, QB, QC, QD, SI, SØ)

U605 (CLR, RS, A, B, C; QA, QB, QC, QD, SI, SØ)

SH4 $\overline{DRCLK}$

U406 (AØ, AI, BØ, BI, CØ, CI, S; QA, QB, QC, QD)

U506 (AØ, AI, BØ, BI, CØ, CI, DØ, DI, S; QA, QB, QC, QD)

U606 (AØ, AI, BØ, BI, CØ, CI, DØ, DI, S; QA, QB, QC, QD)

SH1 $\overline{R2IR3}$

SH8 SYNC1

U109

SGNA SH6,12

MSBA SH6

U305 LSBA SH6

SGNB SH6,12

MSBB SH6

U305 LSBB SH6

DEC OUTPUT SH9,11

U307 SGNC SH7,12

MSBC SH7

U305 LSBC SH7

DEC OUT 1 SH9

U108	74S02
U302	COMP. CARRIER
U305	74LS86
U306	74LS04
U307	74LS08
U308	898-1-R1K
U404	74LS00
U405	74LS194
U406	74LS298

U503	74LS174
U504	74LS157
U505	74LS194
U506	74LS298
U603	74LS174

U604	74LS157
U605	74LS194
U606	74LS298

I/O BOARD SH6

DECODER NODE & PHASE SYNC

FOLDOUT FRAME

U304	74S37
U407	74S472
U408	74S472
U409	74S472
U507	74S472
U508	74S472
U511	74128
U607	74S472
U608	74LS377
U609	74LS377
U610	74LS377
U611	74128
U612	74128
U701	74128
U702	74128
U703	74128

I/O BOARD SH7
DECODER METRIC PROM

FOLDOUT FRAME

FOLDOUT FRAME

VCC — U308 — 13 IE SH8,6,7

VCC — U159 — 16 — 15 14 — 15 14

SH8 IE — 11 12 — U160 Q — 10 — SYNC — J2-5

13 — SYNC — SH9

SYNC1 — SH6

SYNC2 — SH6

U203 — 8 — 9 10 11

U706 — 4 5 — 6

U707 — 1 CL — 4 D — 2 Q — 9

U706 — 9 10 — 8

U804 — 14 13 — Q_A Q_B — 7 P — 10 T — 2 — CL A B C D LD — 1 3 4 5 6 9

U806 — 3 — 4

SH6,15 NORMALIZE

SH8 IE — 1 10 7 — CL T P — U152 — A B C D — C 15 10 T

SH8 IE — 1 7 — CL P — U802 — A B C D LD — C 15 1

U806 — 2

SH8 IE — 1 — U806 — 8

U509 — 6

4 3 2 6 7 — $\bar{E}$ Q_A Q_B Q_C Q_D — 5 $\bar{U10}$ — 14 LD — U803 — D3 — 9

11 — IE — SH8

INTLVR IN — SH4

U806 — 9

U509 — 4 5

U705 — 8 — 11 10 9

R2/R5 1 — 2 — U172 — 3 — 4 5 6 9 2

U172 — 4 5 — 6

4 — U510 — VCC

U172 — 11 — 12 13

U172 — 8 — 9 10

DRCLK — SH4

R2/R3 — SH1

DSCLK — SH4

9 — U503 — D Q — 13 — 12

PI-27 — HARD/SOFTIN

HARD/SFT SH6

TDMA — 14 — 15

PI-22

PI-24

14 15 — U308 — VCC

R2/R3 — SH11

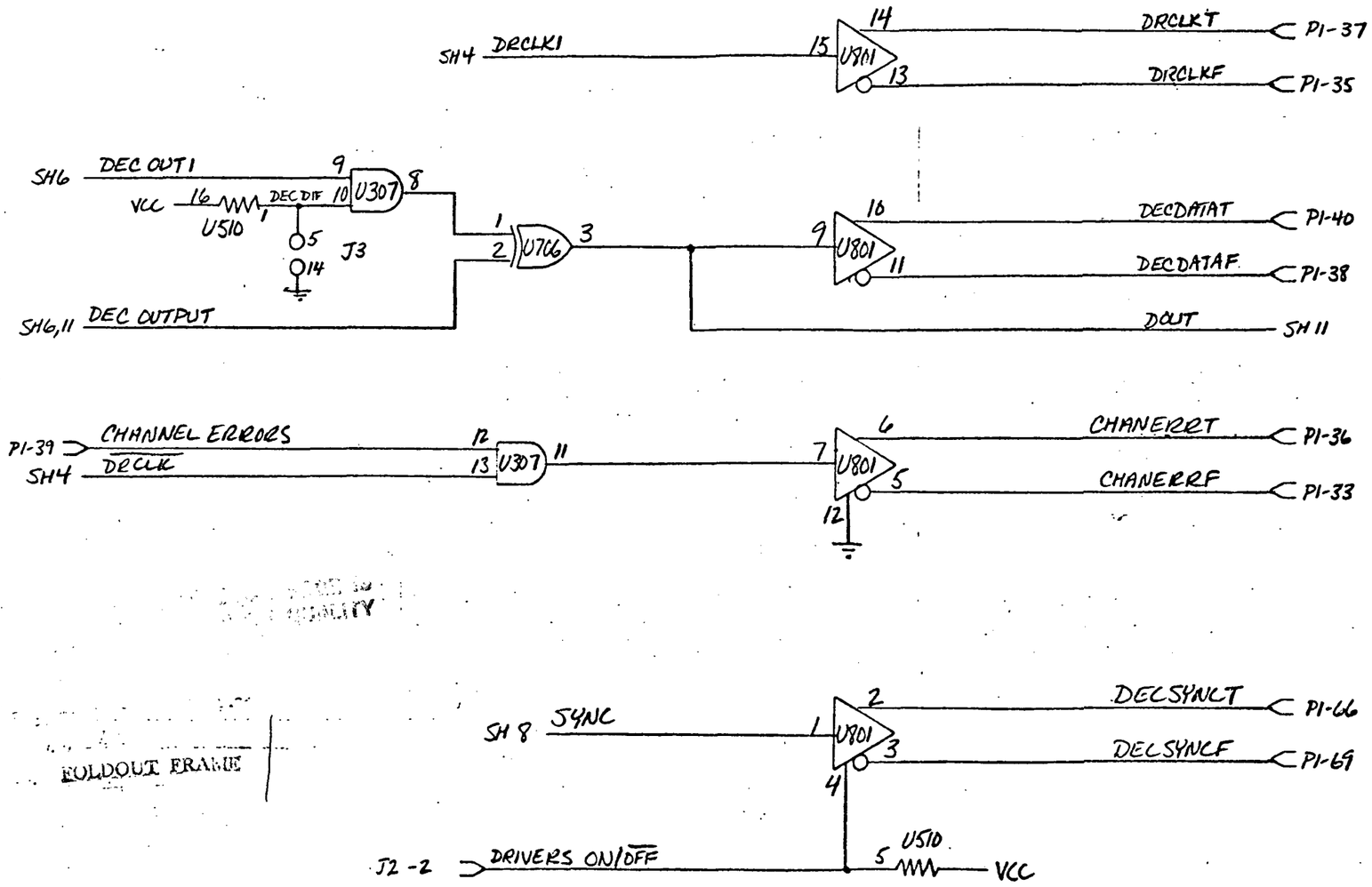
INTLVR IN — SH4

U203	74S10
U308	898-1-R2K
U503	74LS174
U509	74LS08
U705	74LS10
U706	74LS86
U707	74LS175
U802	74LS163
U803	74LS191
U804	74LS163
U806	74LS14
U152	74LS163
U159	COMP. CARRIER
U160	96L02
U172	74LS00

I/O BOARD — SH 8

DECODER SYNC LOSS DETECTION

JUMPER SELECTS NOT DIFFERENTIAL CODING WHEN TIED.

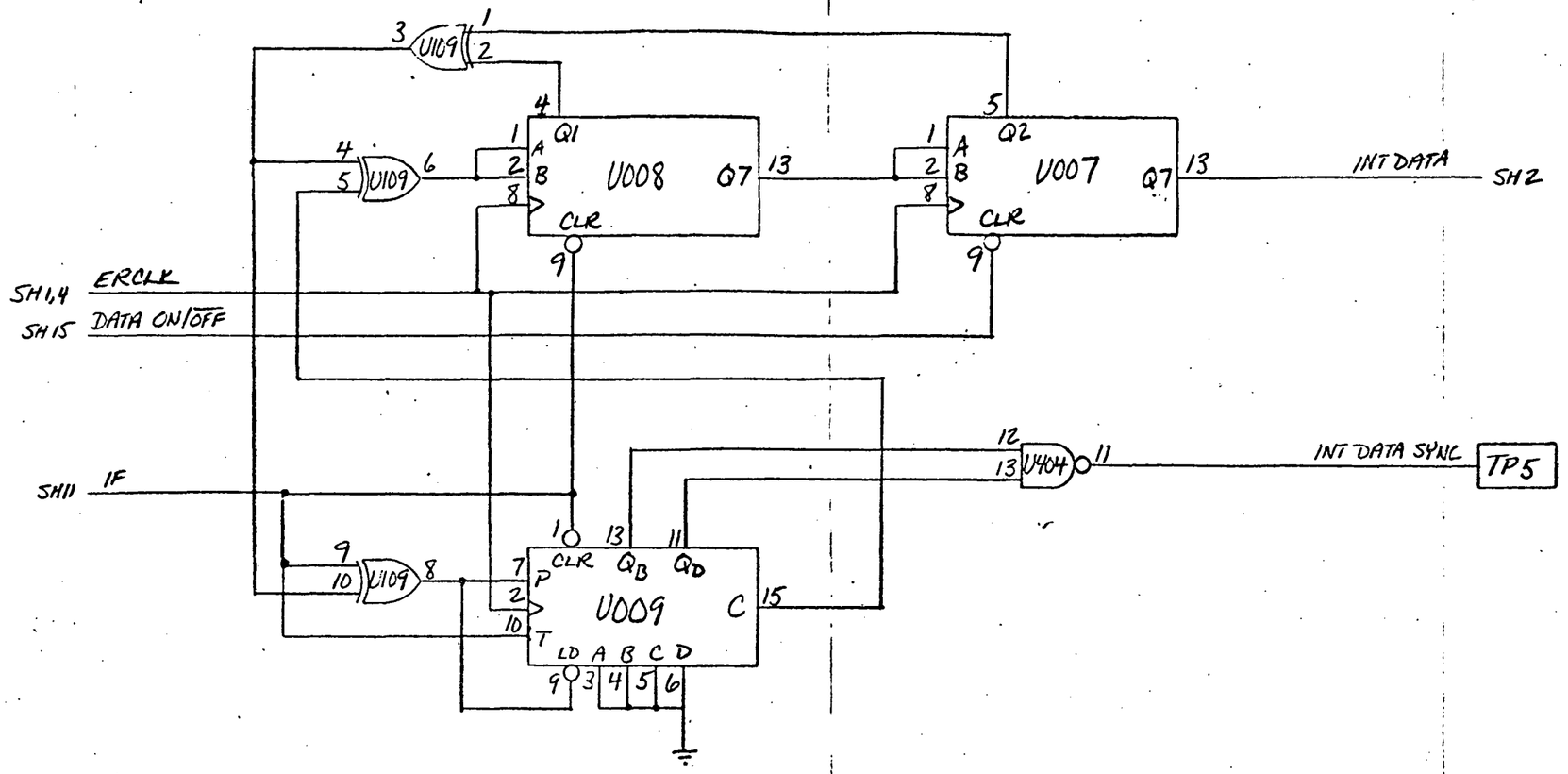


FOLDOUT FRAME

FOLDOUT FRAME

U307	74LS08
U510	898-1-R1K
U706	74LS86
U801	26LS31

I/O BOARD	SH9
DECODER OUTPUT & DIFF. DECODE	



U007	74LS164
U008	74LS164
U009	74LS163
U109	74LS86
U404	74LS00

I/O BOARD SH 10

ENCODER INTERNAL DATA GENERATION

U012	74LS157	U410	74LS74
U109	74LS86	U411	74LS163
U112	74LS00	U412	74LS163
U209	74LS86	U413	74LS153
U210	74LS86	U509	74LS08
U211	74LS164	U510	898-1-R1K
U212	82S129	U707	74LS175
U306	74LS04	U711	74LS04
U309	74LS51		
U310	74LS164		
U311	74LS164		
U313	74LS02		

SH4 DRCLK

SH12 DELAY OUTA

SH12 DELAY OUTB

SH12 DELAY OUTC

SH9 DECODER OUTPUT

SH11 IF

SH11 DOUT

SH4 DRCLK

SH1 $\overline{R2/R3}$

$\overline{DEC\ REV}$ SH7

VCC U510 J3

U211 U212 U209 U109 U306 U309 U310 U311 U312 U313 U410 U411 U412 U413 U509 U707 U711

CHANNEL ERROR SH13,17

OUTPUT ERROR SH13,15

MAX MIN DN/UP

VCC U510 2 IF SH 11,12,13

I/O BOARD SH 11

CHANNEL & OUTPUT ERROR MONITOR

U010	93L422
U011	93L422
U110	74LS163
U111	74LS163
U112	74LS00
U207	74LS86
U306	74LS04
U510	898-1-R1K
U707	74LS175

SH4 DRCLK
SH6 SGNA
SH6 SGNB
SH6 SGNC
U112
IF SH11
U010
U011
DELAY OUT A SH11
DELAY OUT B SH11
DELAY OUT C SH11
U110
U111
U207
U306
U707
SH4 DRCLK
SH11 IF
J3
PATH32
U711
VCC
U510

FOLDOUT FRAME

FOLDOUT FRAME 2

I/O BOARD SH12
ERROR MONITORING – P.M. DELAY COMPENSATION

Row 7

SH 11 IF

SH4 $\overline{DRCLK}$

J2-6 $\overline{CHAN/OUTP\ ERRORS}$

SH9,11, P1-39 CHANNEL ERROR

SH11,15, OUTPUT ERROR

J2-8 10^5

J2-11 $\overline{MAN/AUTO}$

J2-12 GATE

$\overline{CNTR1\ CLK}$ J2-9

AUTO GATE J2-13

$\overline{CNTR2\ CLK}$ J2-10

$\overline{CNTR2\ CLR}$ J2-7

CNTR2 LD J2-17

U708 U709 U710 U711 U712 U713 U714 U806 U807 U808 U809 U810

U708	74LS157
U709	74LS160
U710	74LS160
U711	74LS04
U712	74LS00
U713	COMP CARRIER
U714	96L02
U806	74LS14
U807	74LS160
U808	74LS160
U809	74LS160
U810	74LS160

BOLDOUT FRAME

I/O BOARD SH13

ERROR STATISTICS COUNTER

U014	74LS164
U112	74LS00
U113	74LS164
U114	74LS164
U115	74LS164
U210	74LS86
U213	74LS161
U214	82S129
U215	74LS174
U314	74LS86
U315	74LS298

SH15 NOISE ON/OFF

SH1 INT 2RCLK

SH4 DRCLK

SH8 IE

SH15 SGN ON/OFF

SH1 ESCLK

U014 U115 U114 U113 U213 U214 U215 U315 U210 U314 U806 U112

ISGNØ IMSBØ ILSBØ ISGNI IMSBI ILSBI — SH5

P0A P0B — SH3

IE — SH8

I/O BOARD SH14

CHANNEL NOISE SIMULATOR

SH11,13 OUTPUT ERRORS

SH6,8 NORMALIZE
SH 15 ENORM

J2-34 START

U901 .330 3.3MF U601

U153 U154 U155 U173 U174 U175 U905 U906 U907 U908 U712 U313 U314 U208 U711 U901 U961

FLT SH7

FLT BD1 J2-16
FLT BD2 J2-14
FLT BD3 J2-15
EMUX SH16
S1 SH16
S2 SH16

D0 SH16
D1 SH16
D2 SH16
D3 SH16

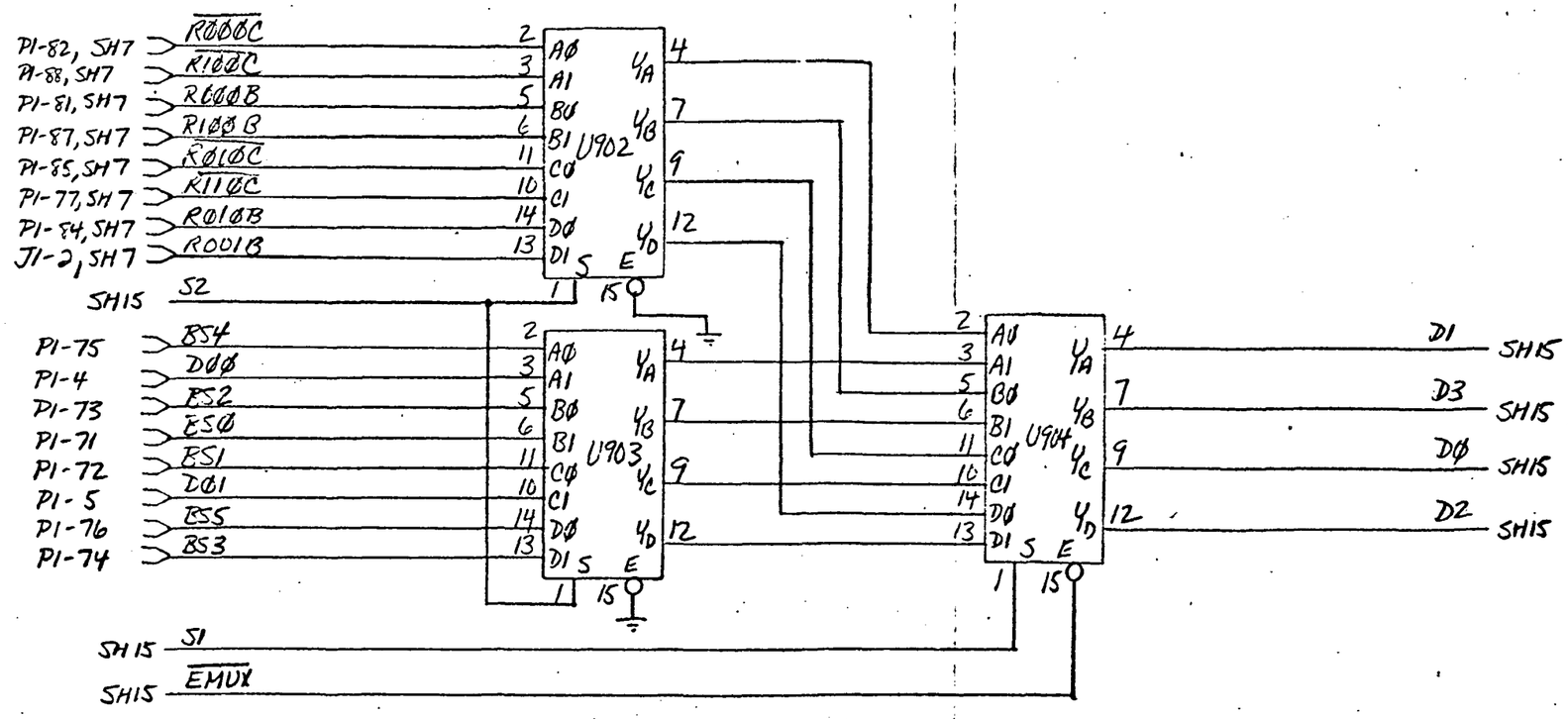
DATA ON/OFF SH10
ENDEH SH15
SGN ON/OFF SH14
NOISE ON/OFF SH14

FOLDOUT FRAME

U208	74S00	U907	74LS138
U313	74LS02	U908	74LS02
U314	74LS86	U153	74LS163
U601	COMP. CARRIER	U154	82S123
U711	74LS04	U155	74LS04
U712	74LS00	U173	74LS163
U901	74LS132	U174	82S123
U905	74100	U175	74100
U906	74100	U176	96L24

I10 BOARD SH15
BUILT-IN-TEST

U902	74LS157
U903	74LS157
U904	74LS157



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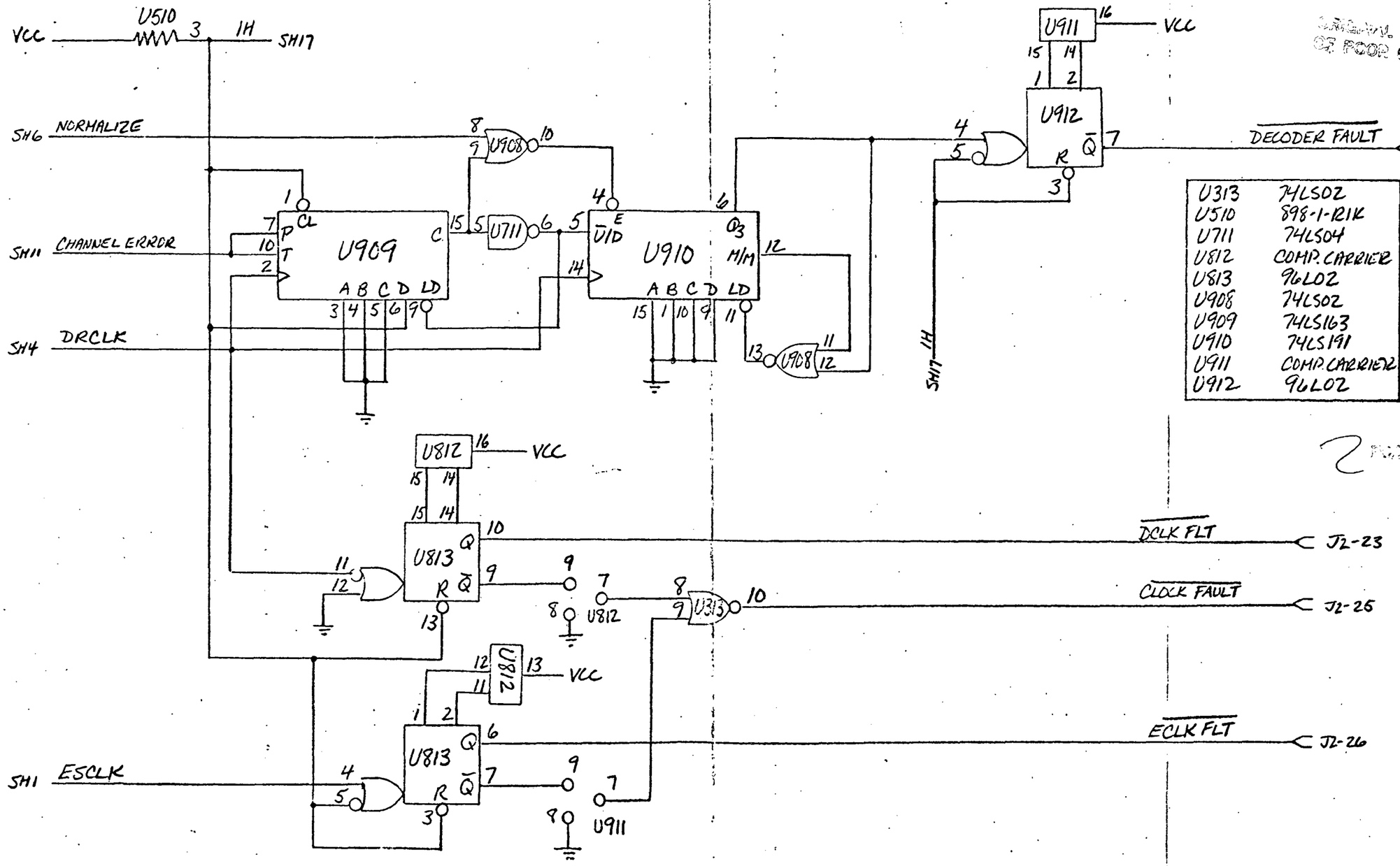
OF POOR QUALITY

FOLDOUT FRAME

FOLDOUT FRAME 2

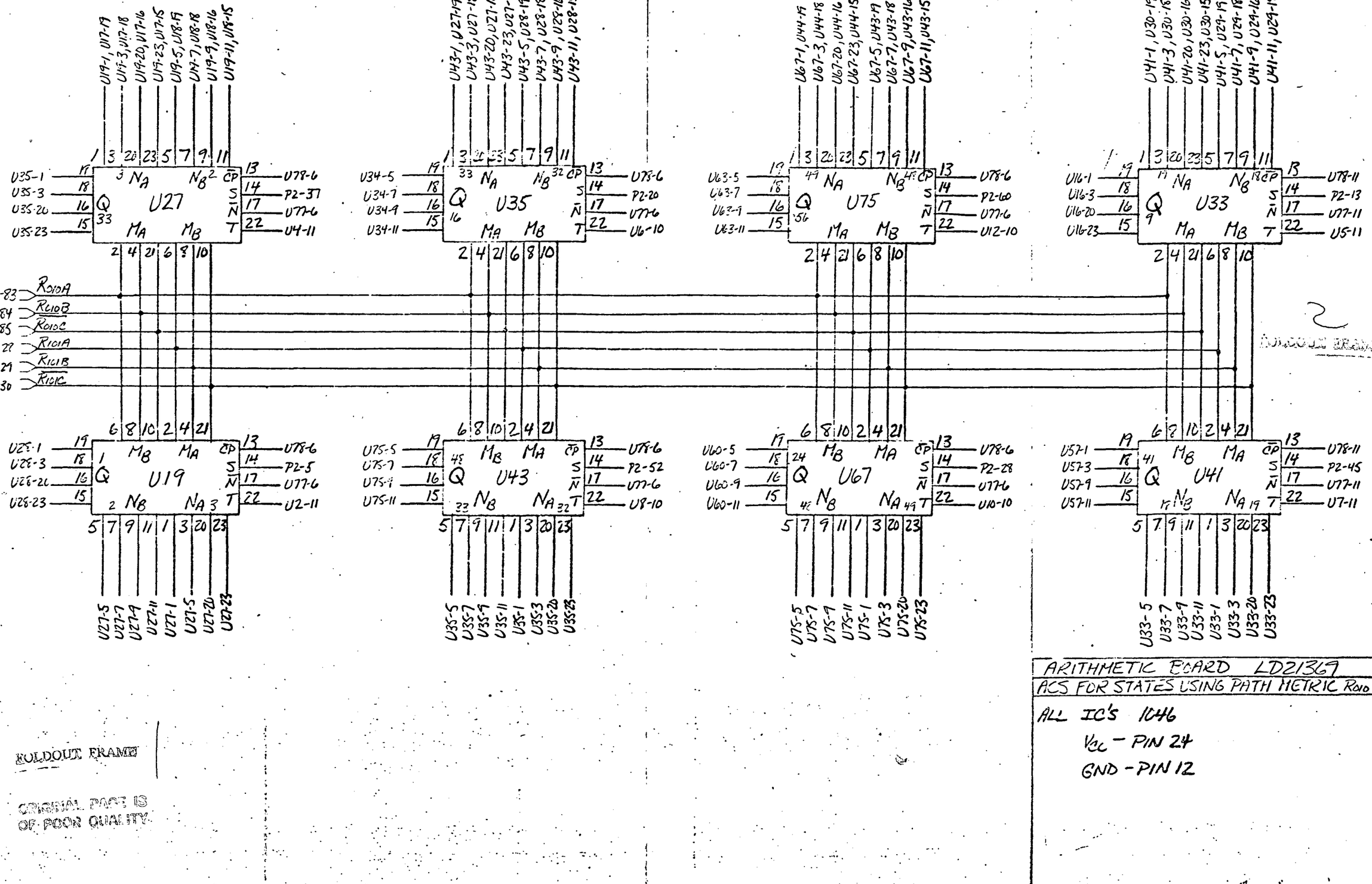
I10 BOARD	SH16
BUILT-IN-TEST	



U313	74LS02
U510	898-1-121K
U711	74LS04
U812	COMP. CARRIER
U813	96L02
U908	74LS02
U909	74LS163
U910	74LS191
U911	COMP. CARRIER
U912	96L02

I/O BOARD SH 17

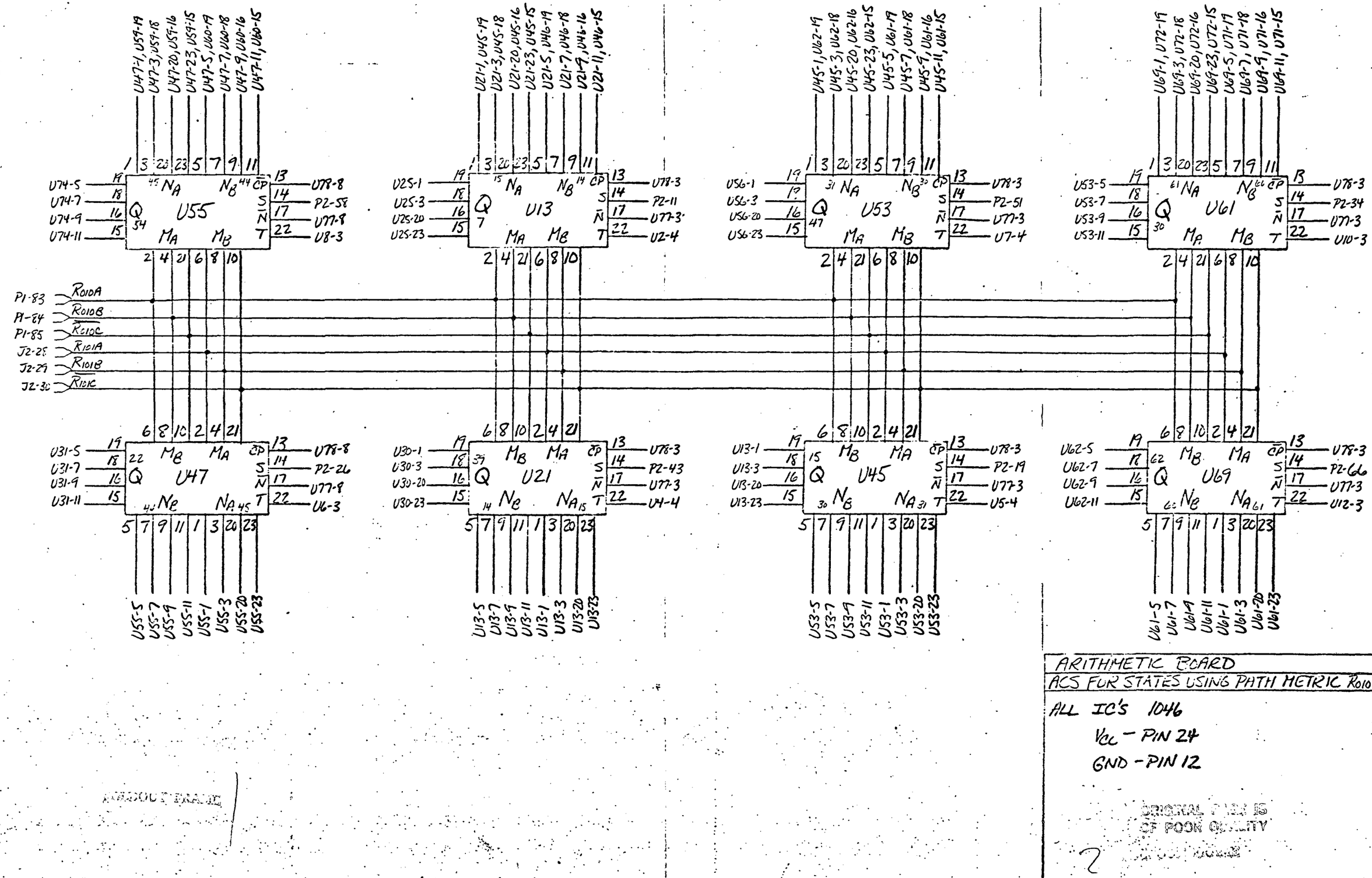
BUILT-IN-TEST FAULT SIGNALS



ARITHMETIC BOARD LD21369
ACS FOR STATES USING PATH METRIC R010

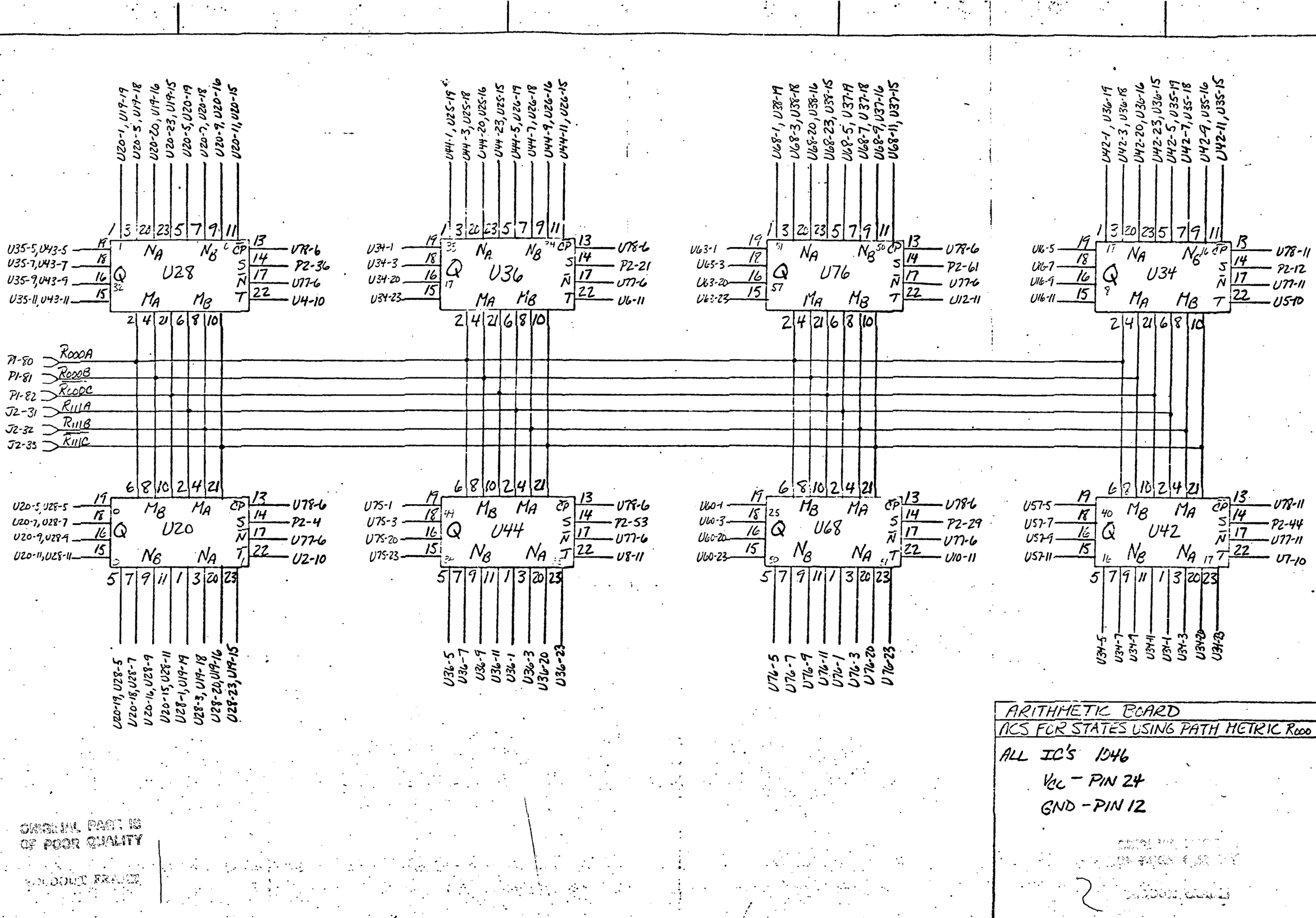
ALL IC'S 1046
V_{CC} - PIN 24
GND - PIN 12

FOLDOUT FRAME



ARITHMETIC BOARD
ACS FOR STATES USING PATH METRIC R010

ALL IC's 1046
V_{CC} - PIN 24
GND - PIN 12



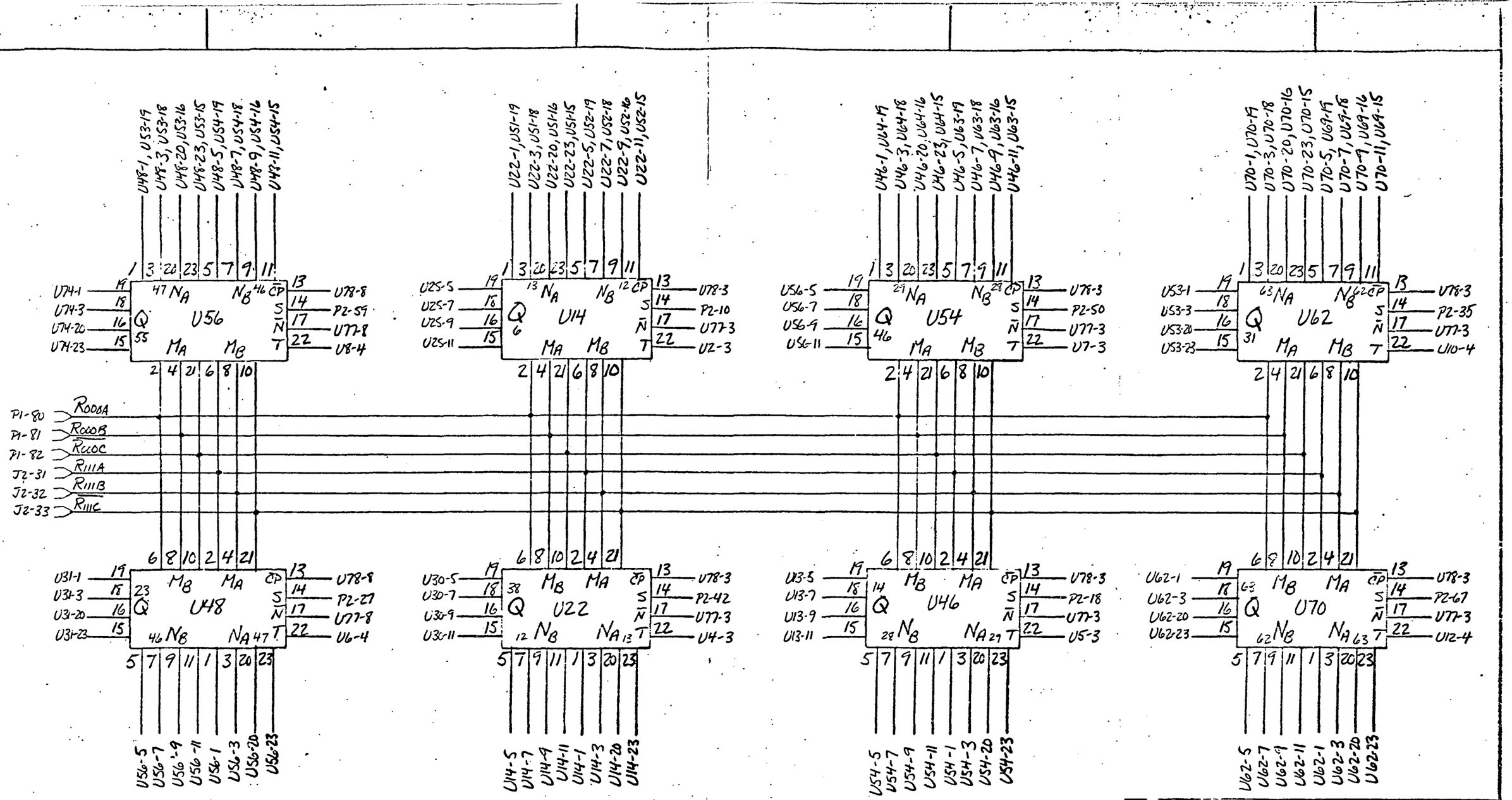
ARITHMETIC BOARD

ACS FOR STATES USING PATH METRIC R000

ALL IC's 1046

V_{CC} - PIN 24

GND - PIN 12



ARITHMETIC BOARD

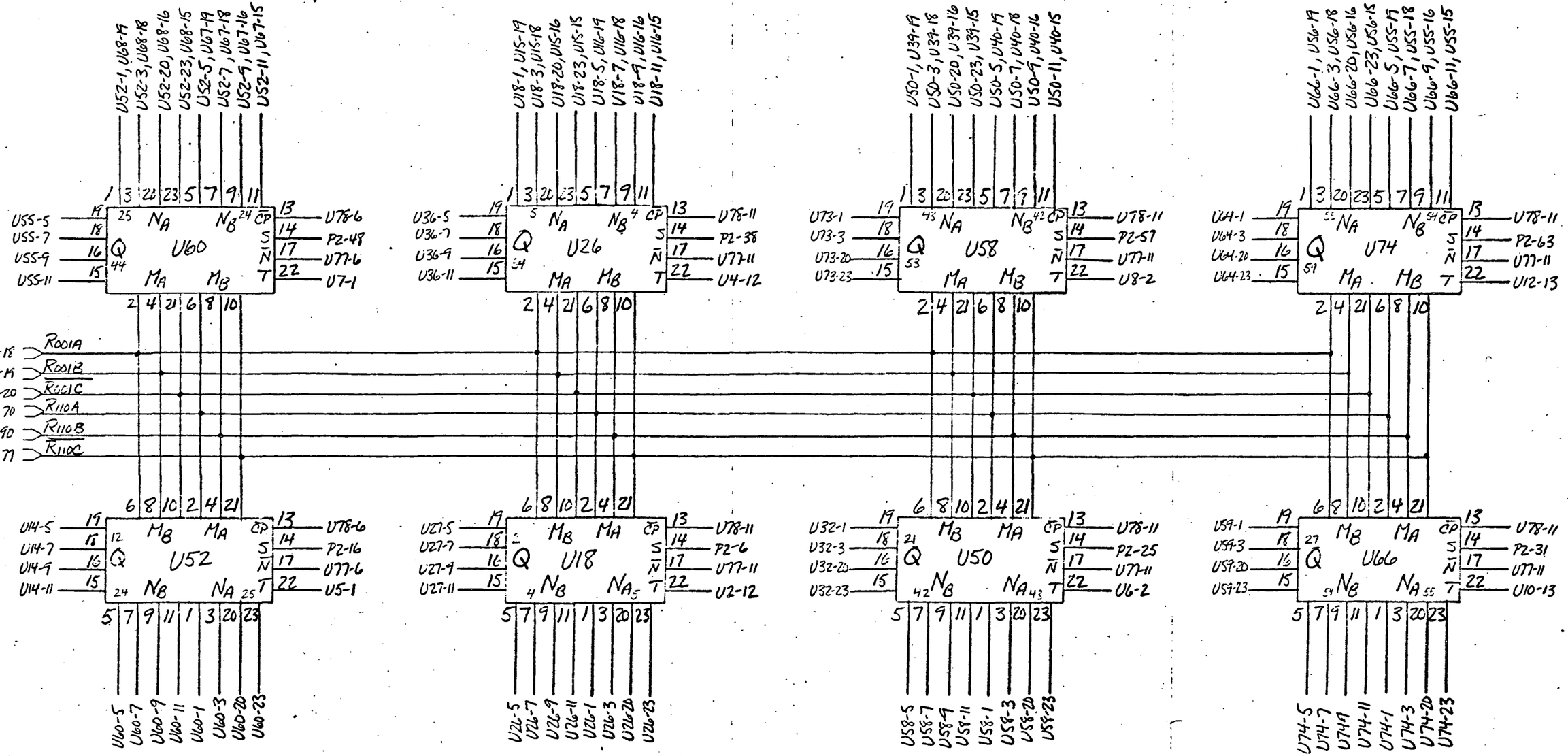
ACS FOR STATES USING PATH METRIC R000.

ALL IC'S 1046

V_{CC} – PIN 24

GND – PIN 12

FOLDOUT FRAME



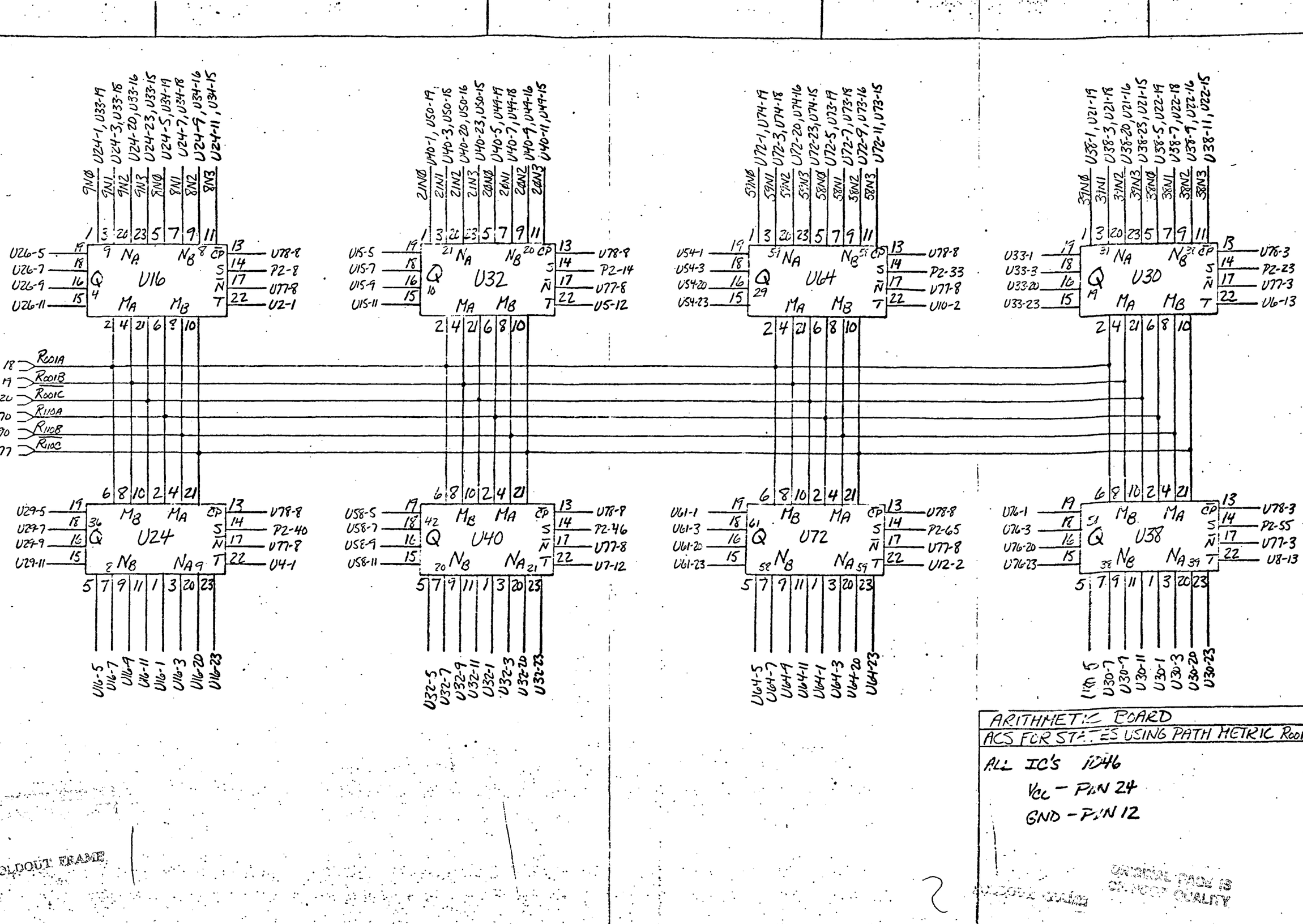
ARITHMETIC BOARD

ACS FOR STATES USING PATH METRIC R001.

ALL IC's 1046

V_{CC} - PIN 24

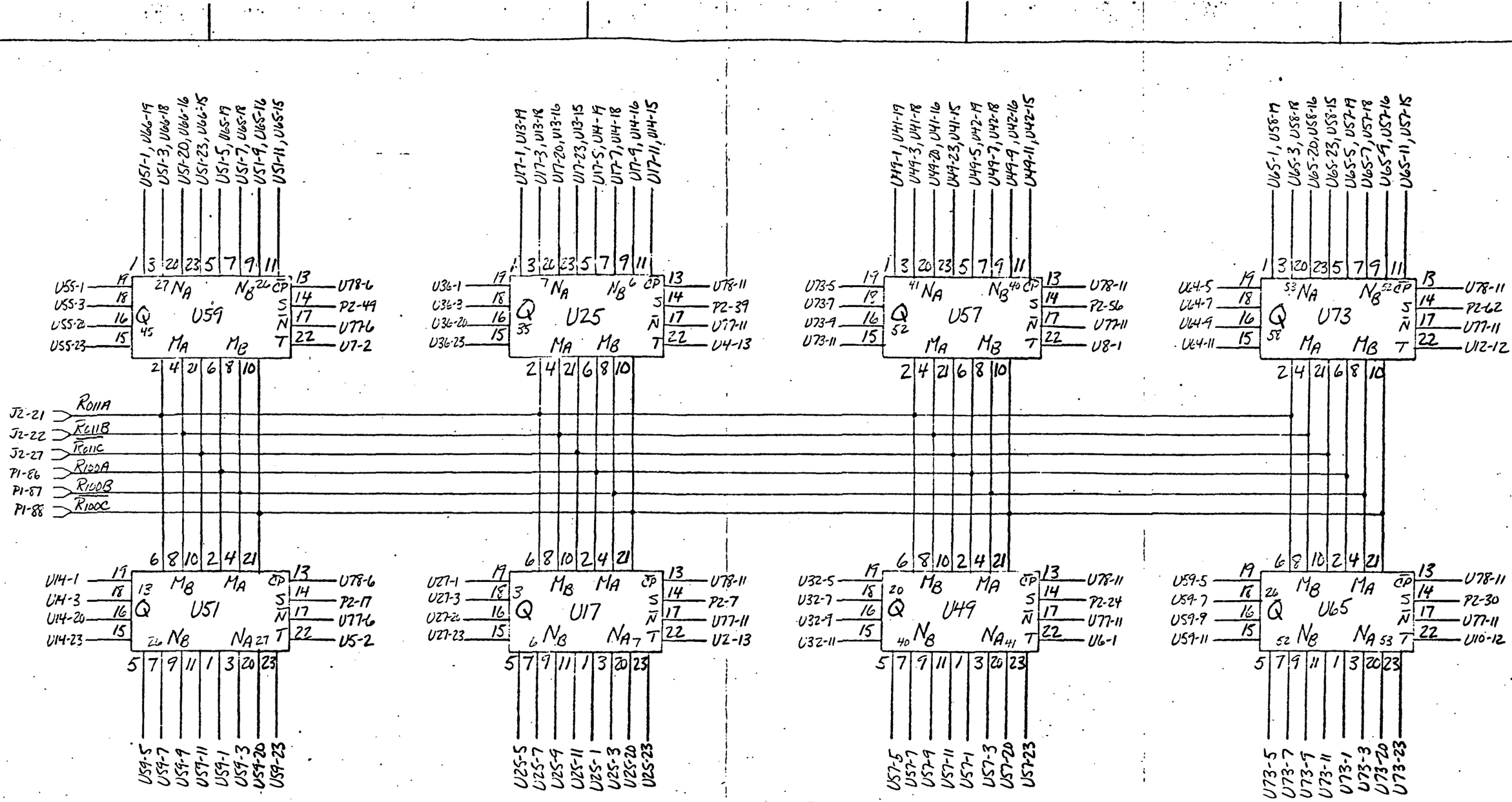
GND - PIN 12



ARITHMETIC BOARD
ACS FOR STATES USING PATH METRIC R001

ALL IC'S 10446
V_{CC} – PIN 24
GND – PIN 12

FOLDOUT FRAME



ARITHMETIC BOARD

ACS FOR STATES USING PATH METRIC R011

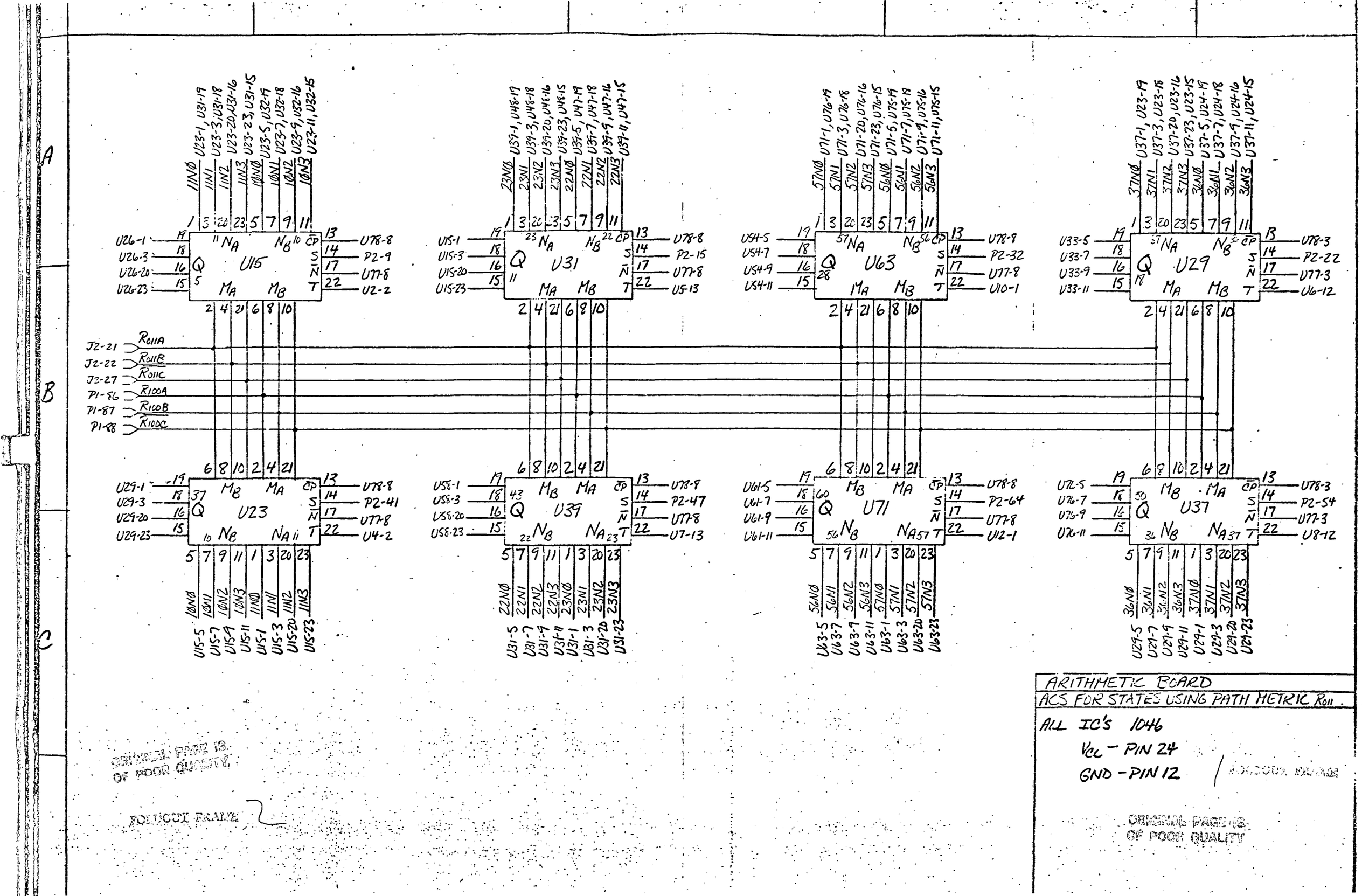
ALL IC'S 1046

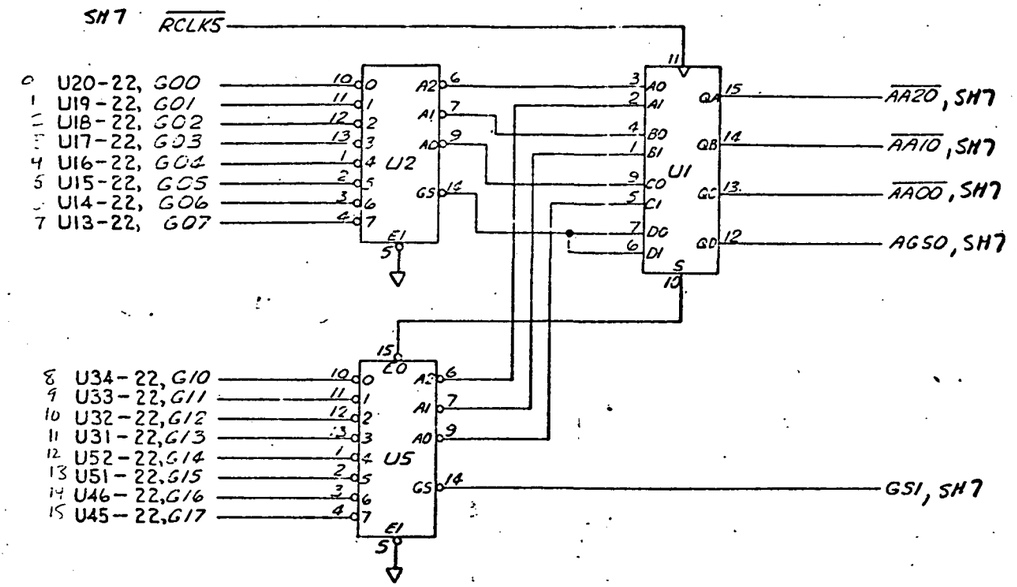
V_{CC} - PIN 24

GND - PIN 12

FOLDOUT FRAME 2

FOLDOUT FRAME


A
B
C
U115
U31
U63
U29
U23
U39
U71
U37
R011A
R011B
R011C
R100A
R100B
R100C
J2-21
J2-22
J2-27
P1-86
P1-87
P1-88
ARITHMETIC BOARD
ACS FOR STATES USING PATH METRIC R011
ALL IC's 1046
Vcc - PIN 24
GND - PIN 12
FOLDOUT FRAME
ORIGINAL PAGE IS OF POOR QUALITY



REF. DES	PART NO
U1	74298
U2	74148
U5	74148

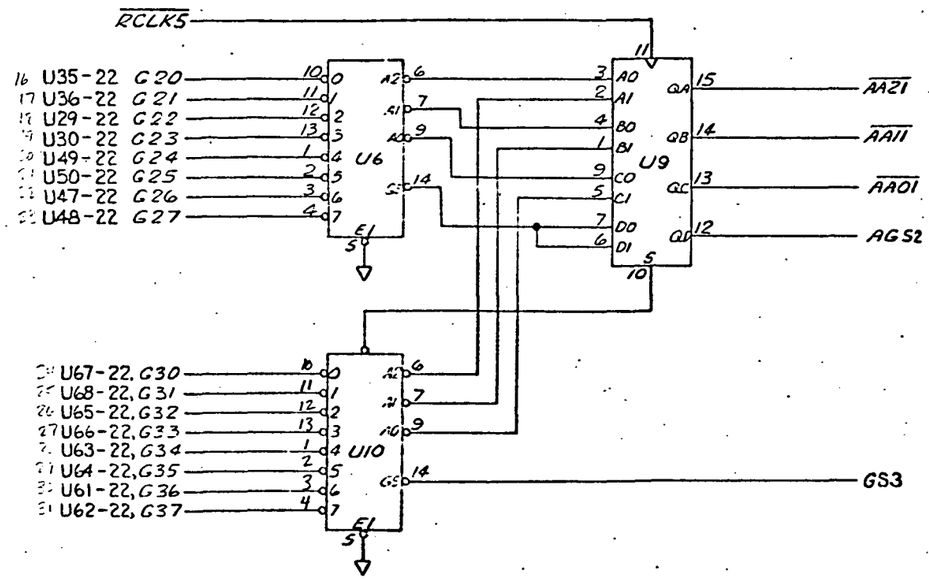
1-

2- ORIGINAL PAGE IS OF POOR QUALITY

FOLDOUT FRAME

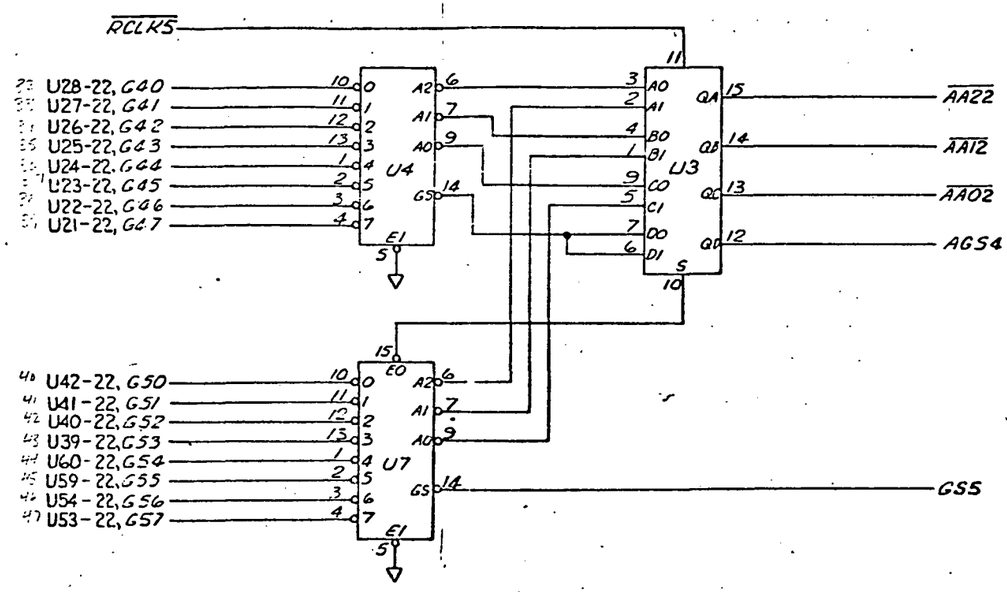
ORIGINAL PAGE IS OF POOR QUALITY

SIZE	CODE IDENT NO	DRAWING NO
C	11627	40 21369
SCALE –	REVISION 5	SHEET 5



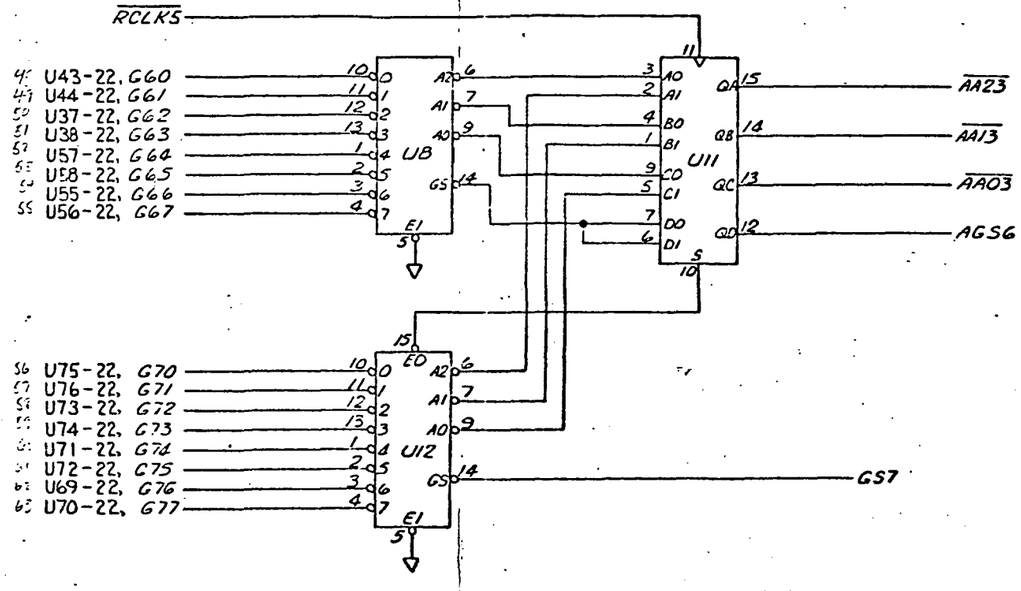
REF. DES.	PART NO.
U9	74298
U6	74148
U10	74148

SIZE	CODE IDENT NO	DRAWING NO	LD21369
C	11627	-	
SCALE -	REVISION B	SHEET 4	



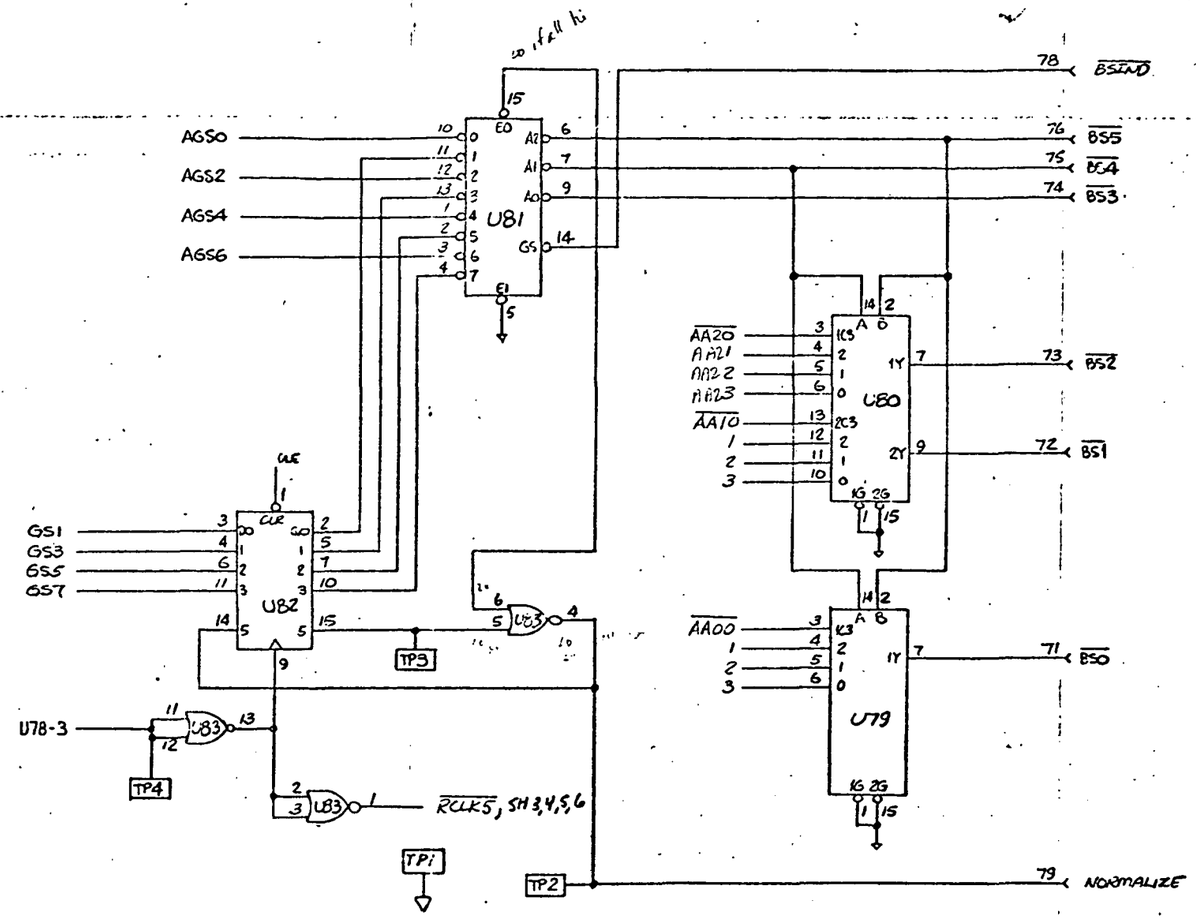
REF. DES.	PART NO
U4	74148
U3	74298
U7	74148

SIZE	CODE IDENT NO	DRAWING NO	LD21369
C	11627		
SCALE —	REVISION B	SHEET 5	



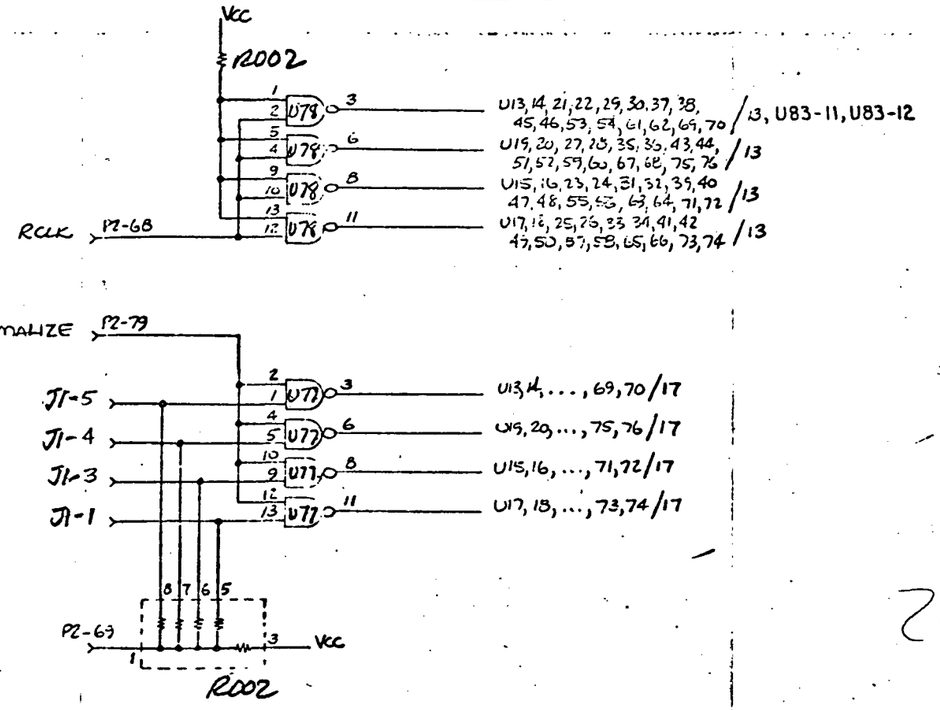
REF DES	PART NO
U8	74148
U11	74298
U12	74148

SIZE	CODE IDENT NO	DRAWING NO
C	11627	LD21369
SCALE --	REVISION B	SHEET 6



REF. DES	PART NO	
U79	74S153	– DUAL 4:1 MUX
U80	74S153	
U81	74148	PRIORITY ENC.
U82	74S174	
U83	74128	

SIZE	CODE IDENT NO	DRAWING NO	
C	11627		LD21369
SCALE –	REVISION		SHEET



REF DES	PART NO
U77	74S37
U78	74S37
R002	COMP. CARRIER

FOLDOUT FRAME

FOLDOUT FRAME

SIZE	CODE IDENT NO	DRAWING NO	LD21369
C	11627		
SCALE —	REVISION B	SHEET 8	

ARITH. PATH MEMORY J1. J10 INTL

+5V

WORD0 WORD1 WORD2 WORD3 WORD4 WORD5 WORD6 WORD7 WORD10 WORD11 WORD12 WORD13 WORD14 WORD15 WORD16 WORD17 WORD20 WORD21 WORD22 WORD23 WORD24 WORD25 WORD26 WORD27 WORD30 WORD31 WORD32 WORD33 WORD34 WORD35 WORD36 WORD37 WORD40 WORD41 WORD42 WORD43 WORD44 WORD45 WORD46 WORD47 WORD50 WORD51 WORD52 WORD53

SGNI+ SGNI- MSBI+ MSBI- LSBI+ LSBI- SGNQ+ SGNQ- MSBQ+ MSBQ- LSBQ+ LSBQ-

TDMA MODE CONTROL

RCLK

DRATE

FRAME+ FRAME-

J2

19 O/QPSK
18 ENCQ/PSK

20 DECQ/PSK
10 DRCLK+
DRCLK-
9 D2RCLK-
7 CHANERS-
23 D2RCLK+
6 DRCLK-
16
22 CHANERS+ D2RCLK+
15 DECDATA-
13
12 DECDATA+
4 ENCIDAT-
3 ENCIDAT+
10 ENCQDAT+
9 ENCQDAT-
1 E2RCLKO-

J3

19 MODEM SGNI+
18 MODEM SGNI-
16 MODEM MSBI+
15 MODEM MSBI-
13 MODEM LSBI+
12 MODEM LSBI-

10 MODEM, DINTL RCLK IN+
9 MODEM, DINTL RCLK IN-
7 MODEM, DINTL 2RCLK IN-
6 MODEM, DINTL 2RCLK IN+
4 MODEM, INTL. DATA OUT-
3 MODEM, INTL. DATA OUT+
1 MODEM, INTL 2RCLK OUT-
37 MODEM, INTL. 2RCLK OUT+

FOLDOUT FRAME

PATH ARITH J1 I/O INTL J3

WORD54 WORD55 WORD56 WORD57 WORD60 WORD61 WORD62 WORD63 WORD64 WORD65 WORD66 WORD67 WORD70 WORD71 WORD72 WORD73 WORD74 WORD75 WORD76 WORD77

J2

37 E2RCLKO+
35 E2RCLKO-
34 E2RCLKO+ EDATAIN+
7
4 E2RCLKI- EDATAIN-
6
3 E2RCLKI+
1 E2RCLKI-
37 E2RCLKI+
35 DSYNC+
34 DSYNC-

RIIA BS0 BS1 BS2 BS3 BS4 BS5 RIIC BSIND NORMALIZE RCCA ROOB ROOC RO1A RO1B RO1C RILA RIOB RIIC GND RIIB GND GND RCLOCK

DECODED OUTPUT

INTL RCLK OUT- 35
INTL RCLK OUT+ 34
INTL SYNCOUT+ 32
INTL SYNCOUT- 31

J1 17 14 11 8 5 2 36 33 30 27 24 21

J2 17 14 11 8 5 2 36 33 30 27 24

FOLDOUT FRAME

-5V